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UNIVERSITY OF ALBERTA

OPTOELECTRONIC REFLEX SIGNAL PROCESSOR

BY

DOBBY LAM

A thesis submitted to the Faculty of Graduate Studies and Research in partial fulfillment of the requirements for the degree of MATER OF SCIENCE.

DEPARTMENT OF ELECTRICAL ENGINEERING

EDMONTON, ALBERTA

SPRING 1994

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January 17, 1994

To my parents who made all this work possible.

ABSTRACT

This thesis describe the design and construction of a reconfigurable optoelectronic signal processor based on a 10x10 optoelectronic switch matrix and 10 replaceable optical fiber delay lines. The overall goal is to demonstrate various signal processing functions, such as switching and filtering, with the processor. This thesis concerns the demonstration of the basic modules and the overall concept. The processor consists of transmitter and receiver modules. The transmitter module with 10 optical transmitters was completed with a bandwidth up to 1.6 GH_Z. Two prototype receivers were built. With the completed portion of the system, various signal processing functions, such as FIR and IIR filtering and cascading switch network, were successfully demonstrated.

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LIST OF ABBREVIATIONS

AC	Alternating current
ACT	Acoustic charge transport
APC	Angled physical contact
APD	Avalanche photodiode
BNR	Bell Northern Research
BW	Bandwidth
CRC	Communications Research Council
CW	Continuous wave
DAC	Digital to analog converter
DC	Direct current
DTSP	Discrete time signal processor
EEPROM	Electrical erasable/programmable random access memory
FC	Fiber connector
FET	Field effect transistor
FIR	finite impulse response
GaAs	Gallium Asenide
I/O	Input/output
IIR	infinite impulse response
MMIC	Monolithic microwave integrated circuit
MSM	metal-semiconductor-metal
O/E	Optoelectronic
OP-AMP	Operational amplifier
PC	physical contact
PIN	Positive-intrinsic-negative
RF	Radio frequency
RIN	Relative intensity noise
Rx	Receiver
SAW	Surface acoustic wave
SDLP	Switched delay line processor
SNR	Signal to noise ratio
THD	Total harmonic distortion
TRLabs	Telecommunications Research Laboratories
Tx	Transmitter
UV	Ultraviolet

LIST OF SYMBOLS

a_n	FIR filter coefficients
b_n	IIR filter coefficients
T_s	Sampling time
$\delta()$	Impulse function
f	Frequency
i	imaginary operator
P_o	Optical power
i_{shot}	Shot noise current
i_{th}	Thermal noise current
I_{ph}	DC photocurrent
i_{g-r}	Generation-Recombination noise current
q,e	Electronic charge
$\{\}$	Spectral density
$\langle\ \rangle$	Root mean square (RMS) value
f_c	3 dB corner frequency
$\Re$	Reflectance
R	Responsivity
B	Bit resolution

1.0 INTRODUCTION

Because of its low loss (<0.22 dB/km) and low dispersion (<17ps/nm/km), optical fiber has been widely recognized for its potential in delay line signal processing applications [1, 2, 3]. However, the high insertion loss of optical switches and the high cost of optical amplifiers restrict the implementation of a reconfigurable optical fiber delay line signal processor. Optoelectronic implementation of a switched delay line processor may be simpler and more practical. An optoelectronic ring resonator using a photoconductor receiver has been demonstrated [4], and a 16 tap transversal filter based on metal-semiconductor-metal (MSM) photodiode array has been exhibited with a programmable bandwidth of 500 MHz [5].

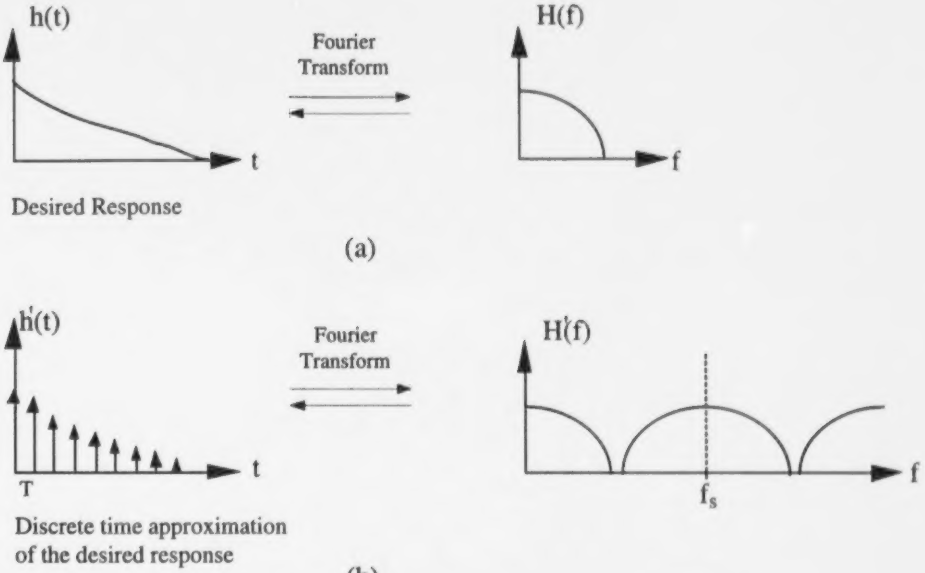
In this thesis, a novel signal processor, which combines optical fiber delay lines and an optoelectronic switch matrix, will be described. This processor is reconfigurable for testing different optoelectronic discrete time signal processing structures such as FIR and IIR in various signal processing applications such as adaptive filters; it can also serve as a switch matrix for broadband signal switching with a high isolation.

1.1 Background

1.1.1 Discrete Time Signal Processing

Discrete time signal processing approximates any arbitrary impulse response by using its discrete time equivalent. Since the impulse response is related to the frequency response by a Fourier transform, a desired frequency response can be approximated by its discretized time impulse response. Figure 1.1 depicts the relationship between the frequency domain representations of a continuous time impulse response and its discrete time equivalent. The discretization is achieved by sampling the continuous function at a regular interval, T_S. Note that the frequency domain representation of the discrete time response is a periodic version of the continuous time response. This periodicity is an artifact of the sampling process. The frequency domain period of the sampled response is $f_S=1/T_s$ where T_s is the sampling interval.

When the bandwidth of the desired response is greater than half of the sampling frequency, the response periods can overlap each other and distort the desired response. This effect is called aliasing. To avoid the aliasing of the response, the sampling frequency, f_S, must be at least twice the bandwidth of the continuous response.



(a)

(b)

Figure 1.1 Relationships between the time impulse and its frequency domain responses. a) A continuous time function and its frequency response b) their discrete time equivalents.

The impulse response of a discrete time signal processor is described by

$$h(t)=\sum_{n=-\infty}^{\infty} a_n \delta(t-nT_s) \tag{1.1}$$

where h(t) is the impulse response of the processor, a_n is the sampled value of the continuous impulse response, which is in general complex, $\delta(t)$ is the impulse function, and T_s is the sampling interval. In theory, the sampling times can be arbitrary and not necessarily equispaced. However, arbitrary sampling times lead to a complicated filter design problem and a periodic sampling interval is normally used to simplify the analysis.

By Fourier transforming Eq.1.1, the transfer function of the series, H(f), is obtained as

$$H(f)=\sum_{n=-\infty}^{\infty} a_n e^{-j2\pi nT_s f} \tag{1.2}$$

which is a complex exponential series with the same coefficients, a_n. It is obvious that the discrete time series can synthesize any arbitrary periodic frequency response within the period $2\pi/T_s$ by applying Fourier decomposition. An arbitrary periodic function, G(f), can be decomposed into a complex exponential series which is given by

$$G(f)=\sum_{n=-\infty}^{\infty} B_n e^{-j2\pi nT_s f} \tag{1.3}$$

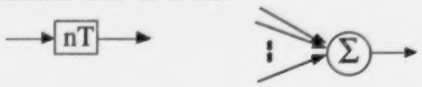
where the coefficients, B_n, can be determined by

$$B_n = \int_{-\frac{1}{2T_s}}^{\frac{1}{2T_s}} G(f) e^{-j2\pi n T_s f} df \qquad (1.4)$$

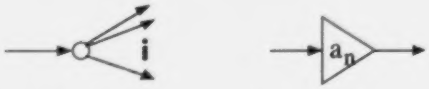
Comparing Eq.1.2 and 1.3 reveals that G(f) can be synthesized with a discrete time series in the form of Eq.1.1 by replacing a_n with B_n. The effects of periodicity in $h'(f)$ can be removed by cascading a low pass filter with a cutoff frequency at half of the sampling frequency to remove the higher order periods. In many real systems, the bandlimited nature of the input signal renders an additional low-pass filter unnecessary.

It can be shown that a time impulse series with an even symmetry is transformed into a real frequency response and an odd series is transformed into an imaginary frequency response [6]. Any complex frequency response can be generated by combining the odd and even time series.

1.1.2 Elemental Components for a DTSP



(a) Delay element (b) Summation element

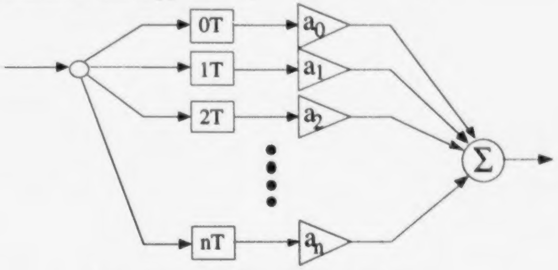


(c) Distribution element (d) Scaling element

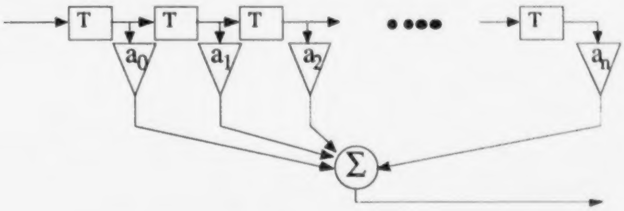
Figure 1.2 Four basic components for a discrete time signal processor

To realize the DTSP structure described by Eq.1.1, we need to employ four basic elements: time-delay, multiplication, branching and summation [1]. Figure 1.2 illustrates these four functions and their block representations. In Figure 1.4(a), nT denotes that the signal is delayed by a multiple n of the incremental delay T. The scaling element (d) scales the output signal with coefficient, a_n. The summing (b) and branching (c) elements perform the signal combining and distribution operations, respectively. By linking and arranging these four elements together, one can realize any transfer function described by Eq.1.1.

The series representation described by Eq.1.1 of the impulse response h'(t) can be synthesized with either the serial tapped delay line or the parallel pipe organ structure shown in Figure 1.3. The input signal is launched into a single delay line or a delay line array with outputs at multiple sampling intervals. Each tapped output is then scaled with a coefficient and all are summed together to form an overall output signal. Each tapped output represents a term in the h(t) series, $a_n\delta(t-nT)$.



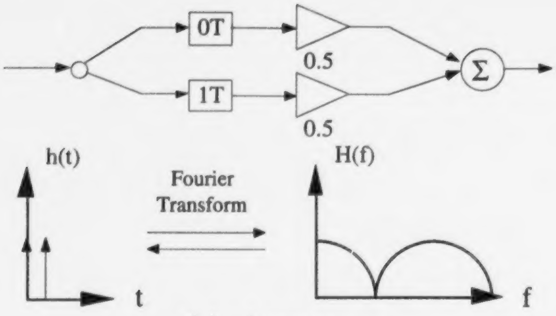
(a) Parallel Implementation



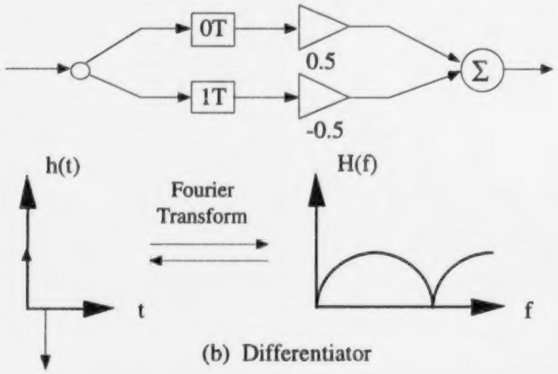
(b) Serial Implementation

Figure 1.3 Two implementations of a FIR structure

The versatility of the discrete time signal processor arises from the fact that different responses can be realized with the same structure using different coefficients. For example, Figure 1.4 shows a single delay structure filter configured as an averager (a low pass response) changed to a differentiator (a high pass response) by modifying the sign of one of the coefficients.



(a) Averager



(b) Differentiator

Figure 1.4 First order averager and differentiator using a two tap FIR filter.

1.1.3 Finite Impulse Response (FIR) And Infinite Impulse Response (IIR)

There are two basic categories of DTSP structures: finite impulse response (FIR) and infinite impulse response (IIR) filter structure. A FIR structure, a truncated implementation of Eq.1.1, is a feed-forward structure in which each tapped delay represents one term in Eq.1.1. The transfer function of an FIR filter structure is given by

$$H(f)=\sum_{n=0}^{M}a_n e^{-j2\pi nT_s f} \tag{1.5}$$

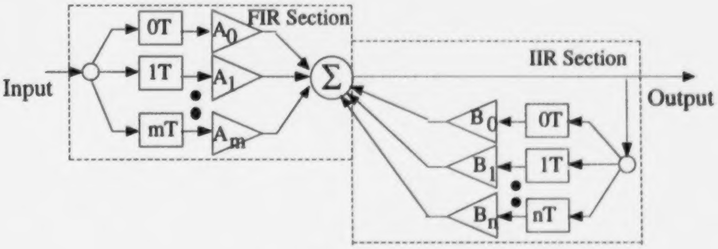
where M is the number of FIR stages. Figure 1.3.a and Figure 1.3.b show the two realizations of a FIR structure: serial tapped delay line and parallel pipe organ structures. The chief advantage of a FIR filter is its unconditional stability. The length of a FIR filter impulse response is always finite; therefore, a FIR filter always satisfies the bounded-in-bounded-out (BIBO) stability criterion [7]. The FIR structure is widely used for adaptive applications, in which the filter coefficients might change over a wide range, to avoid oscillations.

In an IIR filter, a portion of the signal is fed back into the input side of the structure. In general, an IIR filter consists a feed-forward (or FIR) section and a feedback (or IIR section) in series. Figure 1.5 shows two canonical forms of IIR filter. The response of an IIR filter is expressed in the form

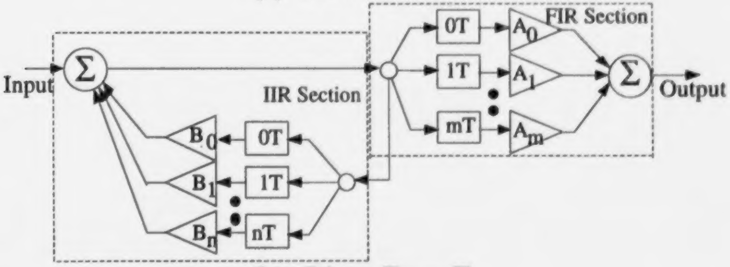
$$H(f) = \frac{\sum_{n=0}^{M} a_n e^{-j2\pi n T_s f}}{1 - \sum_{n=1}^{N} b_n e^{-j2\pi n T_s f}} \tag{1.6}$$

where a_n and b_n are the coefficients for the FIR and IIR sections, respectively [7].

Because of this feedback, an IIR filter can generate an infinite number of impulses instead of a fixed number of impulses. An IIR filter has greater efficiency than a similar FIR filter with the same number of stages; however, this feedback also causes an IIR filter to be potentially unstable with certain coefficient values. This unstability must be considered for any IIR filter design.



(a) Direct Form I



(b) Direct Form II

Figure 1.5 Two canonical forms of IIR filters

1.2 Implementations of the DTSP

Many different discrete time signal processor implementations are categorized by the delay medium used. In Ref.[8], the performances of various delay line technologies, such as charage coupled device (CCD), surface acoustic wave (SAW), acoustic charge transport (ACT), digital electronic, superconductive transmission line, and optical fiber delay lines, were compared in an extensive survey. In terms of the delay tap density, CCD, SAW, and digital delay lines, which are all integrated circuit technology based devices, can provide hundreds of taps on one integrated device. Unfortunately, the bandwidths of these devices are relatively low. Only SAW and ACT delay lines can reach up to 100's of MH_Z. The superconductor delay line has the potential for large bandwidths (2-20 GHz) and potentially long delays due to its low loss. However, the difficulty in broadband coupling and the inherent cooling requirements prohibit any large scale realization of its broadband and low loss potentials. On the other hand, optical delay lines, both in optical fiber form or in an integrated form, can provide a bandwidth potentially up to THz's range and long delay times (10 µs's). The components for implementing broadband and long delay optical fiber delay are commerically available [9].

1.2.1 Optical Delay Lines

Two commonly used optical delay media are optical fiber delay lines and integrated optic delay lines. The optical fiber with its low loss (<0.22 dB/km for monomode fiber) and low dispersion (<1.7 ns/km/nm monomode fiber) is long recognized for its potential in delay line signal processing applications [1,2,9]. The optical loss of high quality monomode fiber commonly used today translates into an electrical loss less than 0.44 dB/km. Propagation delay through optical fiber is about 5 µs/km. The high velocity of light in fiber ($c \sim 2x10^8$ m/s in silica glass) relaxes the constraint on implementing high tap resolution which limits the bandwidth of slow wave delay media such as acoustic wave devices. The high carrier frequency of the optical wave reduces the difficulty in the design of broadband coupling structures which is a major difficulty for the broadband electromagnetic and acoustic delay line [10, 11].

The integrated optic waveguides in various forms, such as ridge, slab, or diffusion types, have a typical propagation losses of fractions of a dB/cm which is considerably higher than optical fiber [12,13,16]. On the other hand, using common lithographic processing, integrated optics offers short, precision time delay down to the picosecond range which is difficult to implement with optical fiber devices [13]. Furthermore, the potential for integrating optoelectronic and optical components, such as lasers and optical couplers, in the same substrate promises the possibility of a monolithic optical delay line signal processor [12, 13]. The high precision delay also allows the application of coherent optical techniques which could generate complex tap coefficients directly by interfering two coherent optical signals [13]. The use of a broadband complex coefficient adds an extra degree of freedom in discrete time signal processor design such as the optoelectronic dispersion compensator described in Ref.[15]. However, the maximum time delay of the integrated optic delay line device is limited by the size of a semiconductor wafer which is constrained to a few inches in diameter. A 1m (~ 5ns delay) long silica integrated delay line coil that occupied an entire 5 inch wafer with only 4 dB loss has been reported [16].

1.2.2 Optical Discrete Time Signal Processor

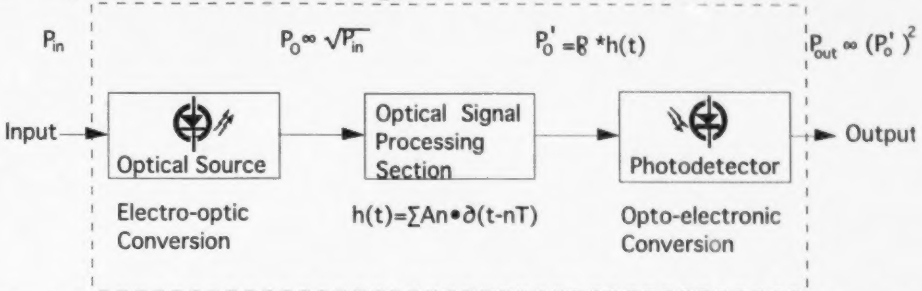

P_{in}
$P_o \propto \sqrt{P_{in}}$
$P_o' = B * h(t)$
$P_{out} \propto (P_o')^2$
Input
Optical Source
Optical Signal Processing Section
Photodetector
Output
Electro-optic Conversion
$h(t)=\sum An \bullet \partial(t-nT)$
Opto-electronic Conversion

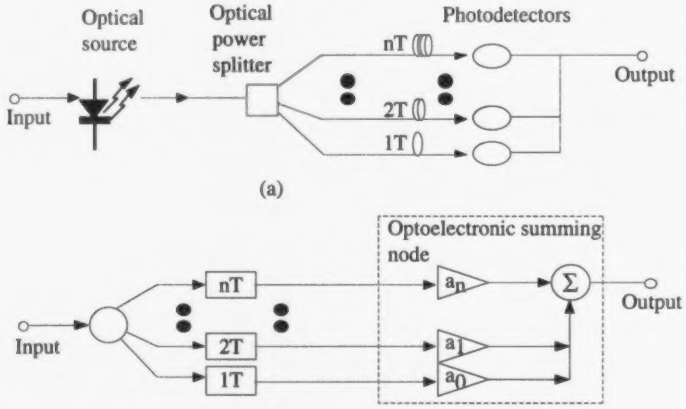
Figure 1.6 A block diagram of a generalized optical signal processor. P_{in} and P_{out} are the input and output electrical power level and P_o and P_o' are intermediate optical power level inside the signal processor.

Figure 1.6 depicts a block diagram of a general optical discrete time signal processor. The input electrical signal is converted into optical form by means of a directly modulated laser diode, or alternatively, an unmodulated laser diode source with an external intensity modulator. The optical signal is then launched into an optical signal processing section where it is manipulated to produce the desired time impulse response function. Inside this optical signal processing section, the optical signal is split, delayed, weighted, routed, and combined to form the desired impulse response. At the output terminal, the optical signal is converted back into electrical output by a photodetector.

In an optical DTSP system, the optoelectronic conversion is confined to the two edges of the system and all the signal processing functions are implemented by optical means. A variety of novel optical techniques, such as microbend adjustable directional couplers [17], fiber V-groove adjustable couplers[18], integrated coherent adjustable couplers [13], and etched fiber reflectors [19], have been developed to implement optical discrete time signal processors. The high coupling loss of these optical devices requires an optical amplification step in order to maintain a reasonable signal to noise ratio. Recently, optical amplification as a weight setting technique and a new class of IIR fiber filter design based on this technique have been proposed[20,21]. The current cost of optical amplifiers, such as erbium doped fiber amplifiers, or semiconductor optical amplifers, is relatively high (~$20,000 for an erbium doped fiber amplifier currently [21]). The cost of the optical amplifier and the losses of adjustable couplers prohibit any large scale implementation of optical DTSP.

1.2.3 Optoelectronic Discrete Time Signal Processor

The major difference between an optoelectronic discrete time signal processor and an optical discrete time signal processor is the usage of optoelectronic conversion in the processing itself. In an optoelectronic DTSP, the optoelectronic conversion is applied to perform two signal processing functions: weighting and summation. Figure 1.7 shows a block diagram of an optoelectronic signal processor in a transversal (FIR) filter configuration. The input signal is converted into optical form by an optoelectronic process as discribed previously. Then the signal is distributed and delayed in an optical form. The scaling and the summing of the intermediate signals into the output signal are performed with an optoelectronic weight setting technique using a photodetector array with a common output bus.



(b)

Figure 1.7 (a) a schematic diagram and (b) a block diagram of an optoelectronic FIR filter

Optoelectronic weight setting modifies the output of a photodetector by electrically modulating its responsivity [1]. The responsivity of a photodetector, such as photodiode or photoconductor, is dependent on its biasing voltage. The biasing voltage controls the carrier transit time, and hence the ratio of transit time to carrier lifetime, that is the photoconductive gain (or attenuation in devices such as photodiodes that do not permit the carrier injection necessary for true photoconductive gain). For a given optical input, the output photocurrent can be scaled by controlling the bias voltage of the photodetector. Figure 1.8 depicts the relationships between the bias voltage and the responsivities of three different types of photodetectors. A unijunction photodiode, such as an avalanche photodiode (APD) or positive-intrinsic-negative (PIN) photodiode behaves asymmetrically under bipolar bias because of its n-p structure. On the other hand, the symmetric structure of a photoconductor or a double junction photodiode, such as a metal-semiconductor-metal (MSM) or Mott photodiode, generates an antisymmetric response under a bipolar bias.

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[1] The responsivity is defined as the ratio between the output photocurrent and the optical power incident on the photodetector.

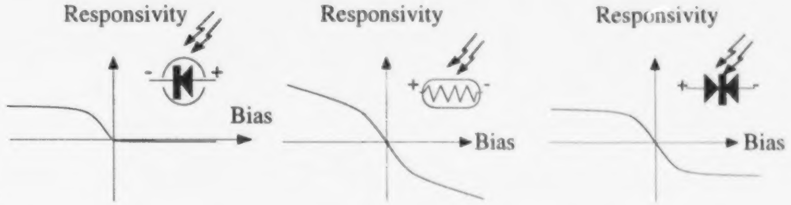


Figure 1.8 The typical photoresponsivities of various photodetectors. A unijunction photodiode, a photoconductor, and a double junction photodiode.

An advantage of optoelectronic weight setting is that the output signals are in the form of photocurrent and can be easily summed together. This summation is accomplished by simply passing multiple intermediate current signals through a common load. A photodetector array with a common output node forms an optoelectronic weighted summing node [22]. By summing photocurrents instead of optical power, optoelectronic summation avoids the addition of temporally coherent signals or spatially coherent signals leading to interference noise. (Incoherent summation of optical signals is not possible. Only mixing can be accomplished.).

1.2.3.1 Historical Perspective of Optoelectronic Signal Processing

The first optoelectronic signal processing was used for switching high frequency signals. Optoelectronic switching in the form of optical gating,with a photoconductor used as an optically controlled switch, was first proposed and demostrated by Auston in 1975 [23]. Optoelectronic weight setting by means of photodetector bias which electrically controls the photodetector responsivity was first demonstrated as a form of switching by MacDonald and Hara in 1978 [22]. Their paper described an optoelectronic switch with an isolation up to 80 dB at a bandwidth of 100 MHz using a PIN photodiode. Figure 1.9 shows the optoelectronic switch described by MacDonald and Hara; the signal switching is accomplished by biasing the photodiode in two states which are formed by applying forward or reverse bias to the PIN photodiode. Subsequently, other devices such heterojunction photodiodes [24], APD [25], and photoconductors [26] had been demonstrated for optoelectronic switching in this sense.

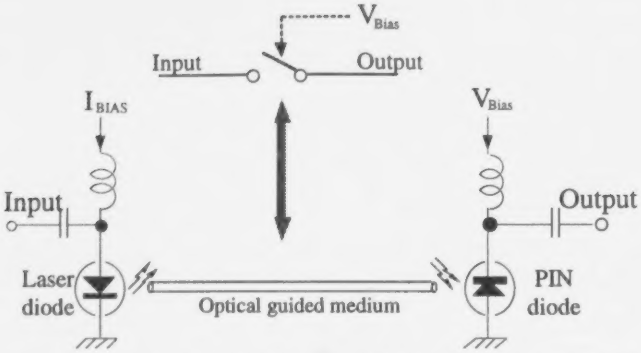


Figure 1.9 The optoelectronic switch using a PIN photodiode. The switching is achieved by completing the optoelectronic signal path using a photodiode bias.

The use of an optoelectronic matrix as a variable delay line was proposed and demonstrated in 1984 [4], using the reflex configuration that is the subject of this thesis. The use of this reflex configuration to perform analog/digital conversion was proposed in 1986 [27], using an optoelectronic continuous weight setting process. Optoelectronic weight setting for signal processing was first demonstrated by Lee [28] in 1991 for an optoelectronic neural network application. An optoelectronic switch matrix with optical fibre delay line as a configurable signal processor was proposed in 1986 in a form of switched delay line signal processor (SDLP) [29]. The first demonstration of continuous weight setting for filtering was demonstrated in an optoelectronic transversal filter experiment [5]. In that experiment, a MSM photodiode array was used to realize a 16 tap transversal filter in a pipe organ (parallel) configuration with a 500 MHz programmable bandwidth.

Up to the present, the experimental results on both optical and optoelectronic delay line signal processors have been based on a predefined configuration. In this thesis, we expand the transversal filter structure used by Swekla [8] into the reconfigurable delay line processor described by MacDonald [29]. MacDonald described a switched delay line signal processor which combines a switch matrix (optical or optoelectronic) with optical fiber delay lines. Figure 1.10 is a conceptual diagram of switched delay line signal processor. This processor can be configured to apply a variety of different signal processing operations such as filtering and code generation either by electronically routing the signal or physically modifying the optical connections.

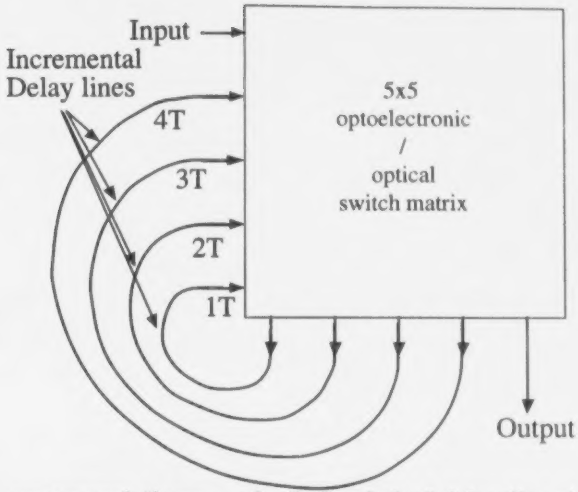


Figure 1.10 A conceptual diagram of a 5x5 switched delay line signal processor

Figure 1.11 is shown an NxM switch matrix which consists of an N dimensional vector of inputs and an M dimensional vector of outputs. The inputs and the outputs are connected via a set of NxM crosspoints; each crosspoint being made up of a switch. Any input can be routed or distributed to any output by closing appropriate crosspoints.

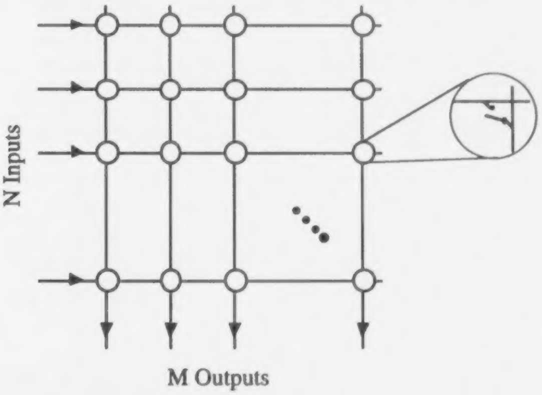


Figure 1.11 A NxM switch matrix

Two crucial requirements for implementing a switch matrix are low crosstalk among the channels and a high isolation between switching states because of the proximity of the input channels and the multiple shared inputs on each output. High isolation and low crosstalk are required to mininize the interference on any output from the unwanted input signals and from adjacent signal paths. These two requirements make optoelectronic switching a suitable technology for high frequency matrix switching. A major advantage of optoelectronic switching over its electrical counterpart is the potentially low crosstalk between channels. By using a guided medium, such as optical fiber, to distribute the optical signal from the light source to the photodetector in conjunction with an electromagnetic shielding, the electromagnetic crosstalk can be reduced to practically zero. An optoelectronic crosspoint with 85 dB isolation has been demonstrated using a heterojunction photodiode [24].

1.2.3.3 Optoelectronic Switch Matrix

In a typical optoelectronic switch matrix shown in Figure 1.12, the inputs are converted into an optical form and each optical signal is distributed into a row of optoelectronic crosspoints. Each crosspoint consists of a photodiode with a control bias. The crosspoint is "closed" or "opened" when the photodiode is sensitized or desensitized to the optical signal input by modulating the bias. The required bias control states are determined by the photodetector type used for the crosspoint. For example, for a PIN diode, forward and reverse biases are commonly used for the "opened" and "closed" states respectively. Each matrix output is formed by summing the photocurrent from a column of photodetectors.

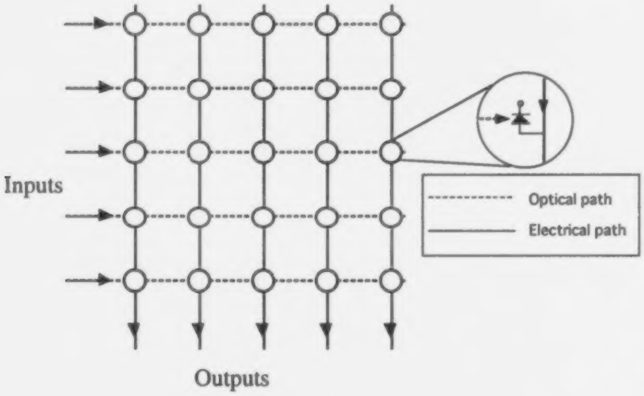


Figure 1.12 a 5x5 optoelectronic switch matrix

A similar 10x10 optoelectronic switch matrix using a novel depletion channel photoconductor array has been demonstrated to have a contrast ratio greater than 60 dB over a 1.8 GHz bandwidth. However, due to the intrinsic properties of depletion channel photoconductor, the crosspoint consistently failed after a short period of operation [30]. In this project, we replace the depletion channel photoconductor with a MSM photodiode which is physically a more stable device and has been demonstrated in many monolithic optical receiver designs. The operation frequency of a single MSM photodiode has been reported up to the 375 GHz range [31].

The MSM photodiode proposed for this project was reported to have a lower isolation (typically 50 dB or less) than the depletion channel photoconductor [30]. The lower isolation of MSM photodiode is chiefly caused by an imbalance in the photovoltages of the two opposed junctions which can be caused by an imbalance either in barrier heights or in the illumination pattern [30]. This imbalance in photovoltage can be partially corrected by applying external bias. Furthermore, the crosspoint isolation can be enhanced by applying additional electronic techniques such as a transmission gate [32] in future integrated versions of the processor.

1.3 Proposed Signal Processor Structure

Figure 1.13 shows a conceptual diagram of the reflex optoelectronic signal processor proposed for this project. The processor is based on a non-blocking switch matrix configuration with input rows and output columns. Each input row is connected to a laser diode which converts the input electrical signal into an optical signal using intensity modulation. This optical signal is launched through an optical delay line and split among 10 fibers using a fiber power splitter. These 10 optical signals represent one input row inside the matrix. One output from each fiber splitter is gathered to form an optical bundle and one of these 10 bundles is fed to each of ten optical receivers. Each optical receiver thus represents an output column from the matrix. Inside the optical receiver, a MSM photodiode array with individual photodiode bias connections acts as a column of crosspoints and a common electrical output bus sums the photocurrents from the entire detector column. An electrical amplifier is then used to compensate for the optoelectronic conversion and optical power splitting losses.

Optoelectronic switching or optoelectronic weight setting is achieved by controlling the bias to each crosspoint. By changing the biasing pattern of the switch crosspoints, one can route, scale, and combine the signals through the switch. By connecting outputs back to inputs with appropriate time delays and by biasing the detectors with appropriate voltages, the switch can be configured to perform different signal processing functions.

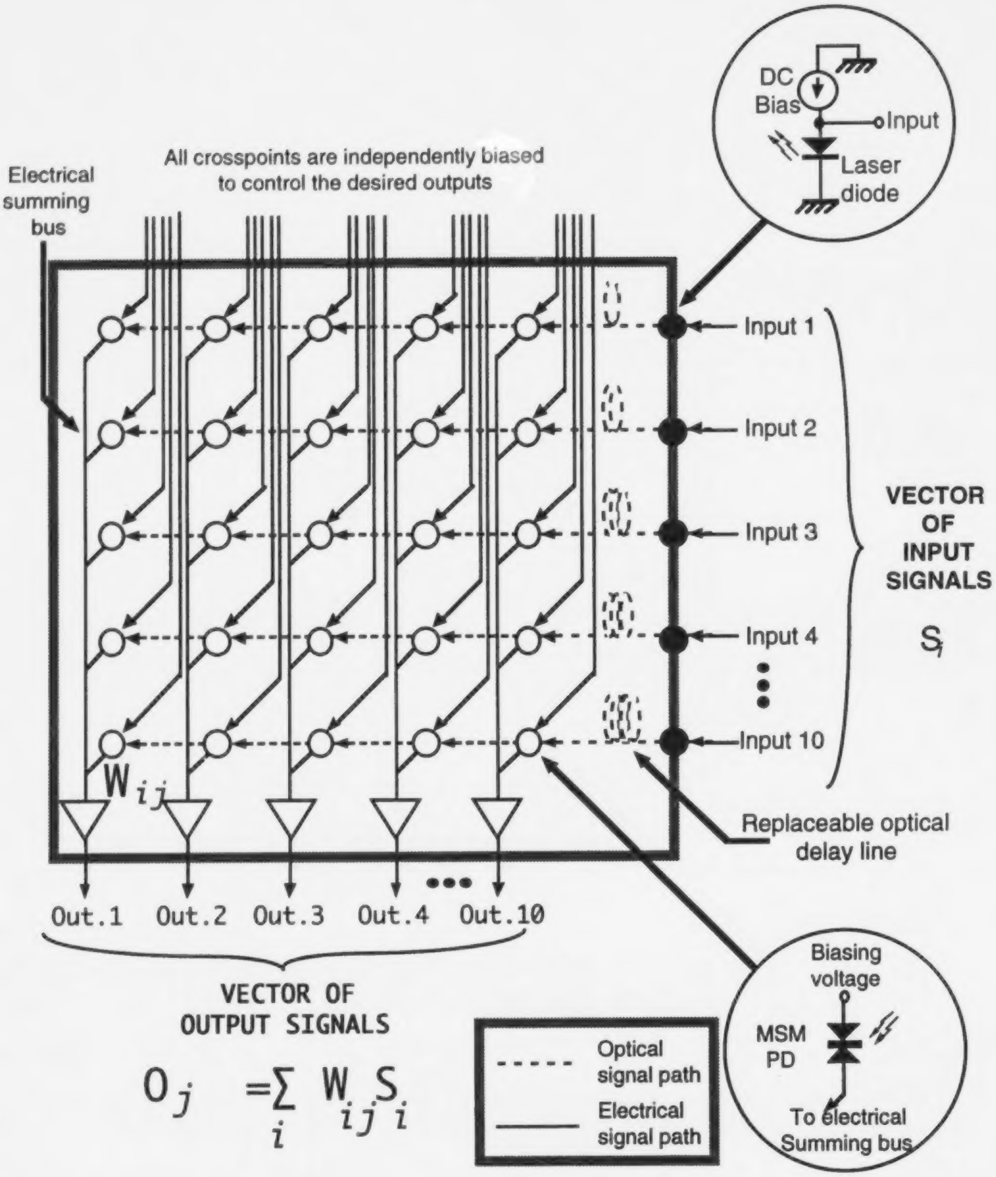
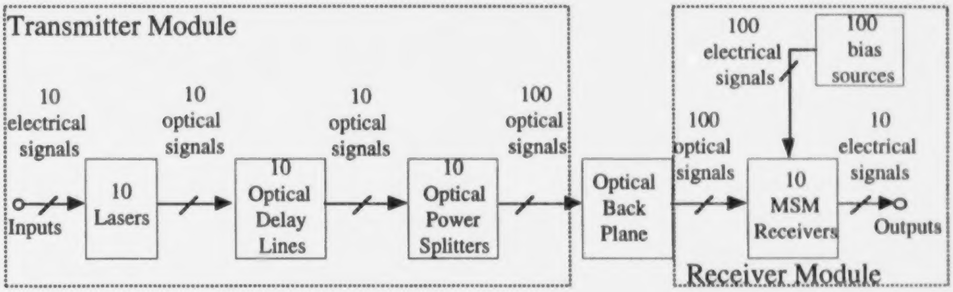

DC Bias
Input
Laser diode
Electrical summing bus
All crosspoints are independently biased to control the desired outputs
Input 1
Input 2
Input 3
Input 4
Input 10
VECTOR OF INPUT SIGNALS
S_i
W_{ij}
Replaceable optical delay line
Out.1
Out.2
Out.3
Out.4
Out.10
VECTOR OF OUTPUT SIGNALS
$O_j = \sum_i W_{ij} S_i$
Optical signal path
Electrical signal path
Biasing voltage
MSM PD
To electrical Summing bus

Figure 1.13 The proposed optoelectronic discrete time signal processor based on a 10x10 matrix

The goals of this project were to construct the reflex optoelectronic signal processor based on a 10x10 optoelectronic switch matrix, to demonstrate the possibility of optoelectronic signal processing, and to study the signal degradation due to circulating the signals through the matrix.

Figure 1.14 shows the organization of the proposed processor. The processor divides into two modules: transmitter module and receiver module. These two modules are linked with an optical backplane. The transmitter module represents the 10 input rows of the matrix; it converts the 10 electrical inputs into 100 delayed optical signals to illuminate 100 crosspoints. The receiver module represents the output columns of the matrix; it converts the optical signals back into 10 electrical outputs according the crosspoint biases. 100 programmable bias sources in the receiver module are used to generate 100 crosspoint biases.



Transmitter Module
10 electrical signals
Inputs
10 Lasers
10 optical signals
10 Optical Delay Lines
10 optical signals
10 Optical Power Splitters
100 optical signals
Optical Back Plane
100 optical signals
100 electrical signals
100 bias sources
10 MSM Receivers
10 electrical signals
Outputs
Receiver Module

Figure 1.14 The organization of the proposed processor

1.4 The organization of the thesis

In Chapter 2, the performance of the proposed system in various applications is estimated based on the available components and the configuration used. In Chapters 3 and 4, the detailed structures and performances of the switch modules are presented. In Chapter 5, the performance of the processor for different signal processing functions is investigated and results are presented. In Chapter 6, a summary of the completed portion of the processor is presented and future experimental directions are described.

2.0 SYSTEM CONSIDERATIONS

In this chapter the components of the reflex optoelectronic signal processor are described. The performance of the processor with available components is estimated and some requirements of the processor for various applications are examined and estimated.

2.1 Component Performance

The performance of the processor is determined by its components. Four major components which dictate the system performance are the photodetector array, receiver amplifier, laser diode, and fiber optic elements. In this section, we examine the characteristics of these components and their impacts on the system performance.

2.1.1 Metal-semiconductor-metal (MSM) photodiode array

The heart of the optoelectronic switch matrix is the crosspoint photodetector array which determines the isolation and the bandwidth of the crosspoints. The photodetector used in this project is a MSM photodiode array. Figure 2.1 shows a MSM photodiode which consists of a double Schottky contact structure on a thin epitaxial layer of intrinsic Gallium Arsenide (GaAs) grown on a semi-insulating GaAs substrate. The thin epitaxial active layer confines the photogenerated current to flow within the high electric field surface region which enhances the speed of the photodiode. The double Schottky contact of a MSM detector eliminates low frequency photoconductive gain, as seen in photoconductors, by blocking carrier re-injection [33]. The double Schottky barrier also reduces dark current which ranges from hundreds of nA to less than 1nA depending on the Schottky contact [34, 35]. A single MSM detector with a bandwidth of 375 GHz and a dark current of 300 nA operating at 8V has been reported [31].

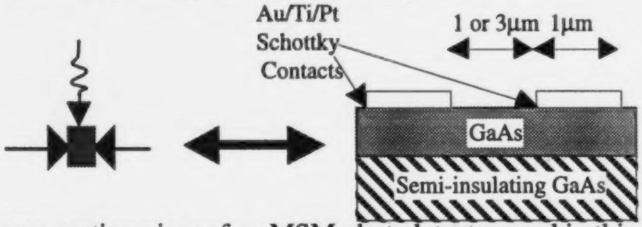


Figure 2.1 A cross-section view of an MSM photodetector used in this project and its circuit equivalent

The symmetry of the MSM photodiode allows biasing with either polarity, making possible either positive or negative photocurrent from a single detector with one optical input. This bipolar sensitivity permits bipolar weight setting, which is required for some signal processing operations, such as differentiation and subtraction [36]. Other optical/optoelectronic signal processors require either two separate, parallel weight setting subsystems for positive and negative weights [1,20,29] which causes an additional 3 dB optical loss, or a coherent optic system which requires a narrow linewidth and highly stable source, to generate bipolar weights [13].

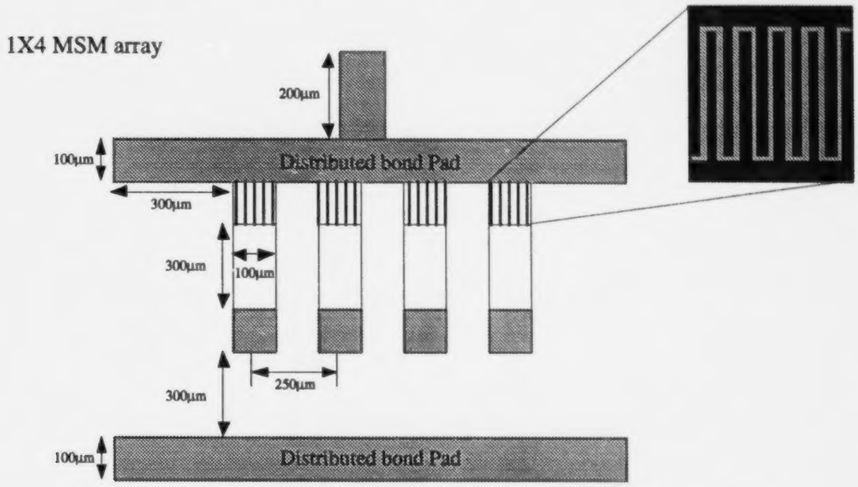


Figure 2.2 A schematic diagram of the 1x4 MSM detector array

Figure 2.2 shows a drawing of the MSM photodiode array used in this project. The detector was designed by Rohit Sharma of the Telecommunications Research Laboratories (TRLabs) and was fabricated by Bell Northern Research (BNR) in Ottawa, Canada [37]. The pitch of the detector array is 250 µm center to center, chosen to be compatible with the standard optical fiber ribbon cable. Photodiodes with two different finger spacings, 3µm and 1µm, and different sizes arrays (1x4, 1x8, and 1x12) were fabricated for different responsivities and bandwidths. The frequency responses of these detectors in parallel was confirmed to be above 1.6 GH$_Z$ at TRLabs. This measurement was limited by the optical source bandwidth. The bandwidth of a single detector was measured to be 4.5 GH$_Z$ at CRC [38], using a wideband optical source. The photodiode with 1µm finger spacing was selected for this project because it exhibited a higher bandwidth than the 3 µm spacing photodiode during the initial testing.

The relationship between the bias voltage and the frequency response of a 1 µm MSM detector is illustrated in Figure 2.3 which shows the isolation between ON state (5V bias) and three different OFF states. The three different OFF state conditions are open circuit bias, 0 V (short circuit) bias, and 12.7 mV bias[2]. Note that the highest isolation occurs when the OFF state is an open circuit, or when the photodiode is biased slightly above zero voltage, rather than 0V bias. The requirement for an offset voltage to achieve minimal sensitivity may be explained by an imbalance of the photovoltages of the two junctions. Under open circuit bias, the residual photocurrent is eliminated by the high series impedance of the open circuit and thus the output current is dominated by the noise floor of the measurement setup.

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[2] This value varies from detector to detector.

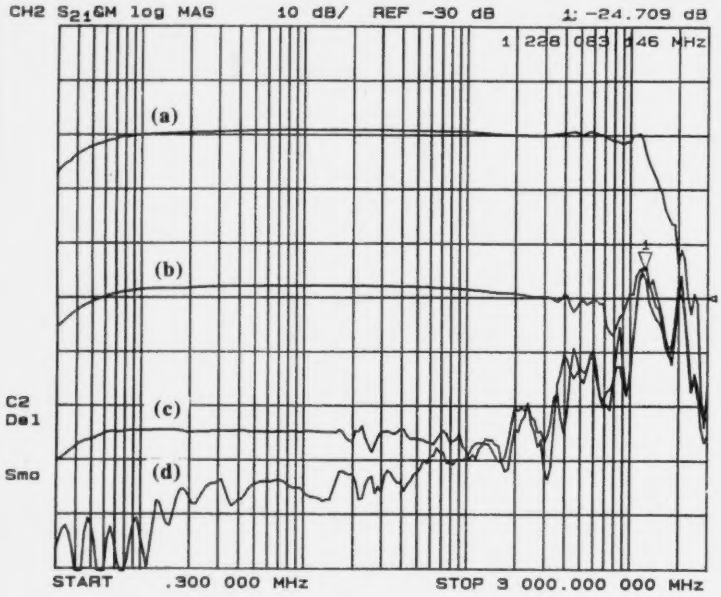

Figure 2.3 The frequency response of a 1μm MSM detector under different biasing conditions. $P_0 = 410\ \mu W$. The bias conditions are (a) 5V, (b) 0V, (c) 12.7mV, and (d) open circuit. The output is amplified with a 56 dB amplifier.

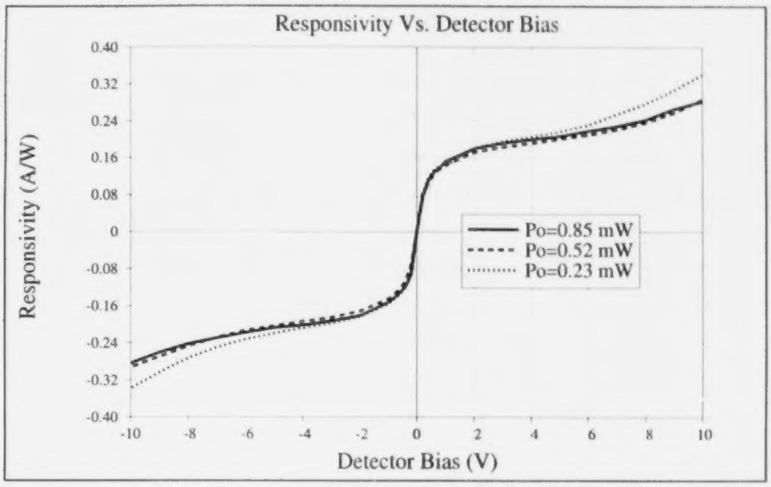

Figure 2.4 The DC response of 1 μm photodiode under different bias voltages and optical powers.

Figure 2.4 shows the DC response of a 1 μm detector with different biasing voltages and optical powers [39]. When the detector is under a high bias, the dc responsivity of the detector is in excess of the theoretical[3] predicted value of 0.21 A/W . This apparently indicates a gain caused by high applied fields. Because Schottky barrier height can be lowered under an intense electric field [40], there may be carrier re-injection at high bias, permitting photoconductive gain.

Figure 2.5 shows the relationship between the detector bias and the output signal recorded with a modulation frequency of 200 MHz. Note that this relationship is not exactly symmetric which might indicate an imbalance of the Schottky contacts or an imbalance in the DC photovoltage. This would also explain the offset bias required to extinguish the crosspoints. Saturation of the output signal was observed at a bias greater than 2 V.

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[3] See Appendix I for detailed responsivity calculations.

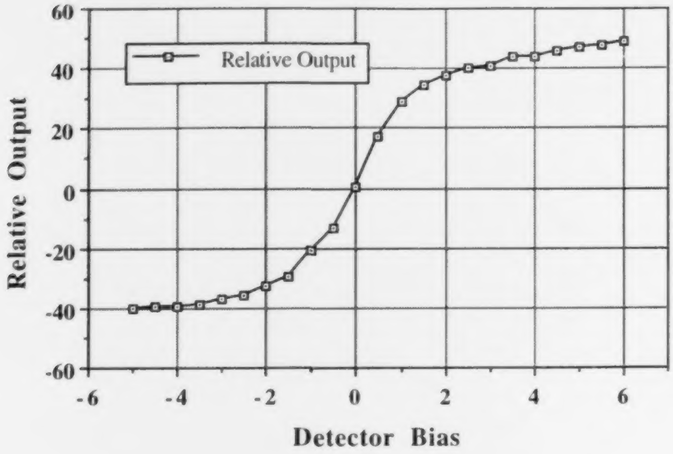

Figure 2.5 The AC response of a 1 µm MSM photodiode as a function of bias. f=200MHz. Po=410 µW.

2.1.1.1 Detector noise

The detector noise is a major factor influencing system performance. There are three major noise mechanisms for the MSM photodiode: shot noise, thermal noise, and generation-recombination noise [41].

When a current flows across a potential barrier , the individual carriers cross the barrier independently and at random. This random process gives rise to shot noise. Assuming a constant noise distribution over frequency, the mean square shot noise current corresponding to a given DC current I is given by [42]

$$\left\langle i_{shot}^{2}\right\rangle = 2qIBW \tag{2.1}$$

where q is the electronic charge and BW is the bandwidth.

There are two current components in every photodetector: dark current and photocurrent. In a photodetector, the dark current is the current portion present when the detector is not illuminated. This current is due to leakage through the barrier or the device surface [41]. The exact value of this leakage is determined by the properties of the metal-semiconductor interface and the bias voltage level. The dark currents of different samples tested vary from microamperes (10^{-6} A) to not observable.

The photocurrent shot noise, also known as current noise, is the shot noise caused by the average signal current [41]. Based on a responsivity of 0.2 A/W and an incident optical power of 500 µW, the DC photocurrent is expected to be on the order of 100 µA which is significantly larger than the dark current; therefore, the photocurrent shot noise dominates the shot noise contribution. A study with similar MSM devices has shown that the dark current can dominate the shot noise contribution under an extremely high bias voltage (~ 50 Volts) [34].

Based on an AC responsivity about 0.2 A/W and an average detector optical power of 500 μW, the shot noise current density is calculated to be in the order of 6 pA/√Hz.

Thermal noise, also known as Johnson noise, is associated with the fluctuations of the thermal velocities of free charge carriers. The mean squared noise current is given by

$$\left\langle I_{th}^{2} \right\rangle = \frac{4kTBW}{R_{eq}} \tag{2.2}$$

where T is the absolute temperature of the device and R_{eq} is the equivalent resistance of the device. The high dynamic impedance of a MSM photodiode, which is commonly modeled with a gigaohm (GΩ) resistor [43], diminishes the thermal noise term to an insignificant level. Based on a 100 MΩ equivalent resistance model, the thermal noise of a MSM diode is estimated at ~400 fA/√Hz.

The generation-recombination noise is due to the random fluctuations in the number of free charge carriers generated through traps . The processes of capture and of re-injection of charge carriers are accelerated with an increase in temperature and with the absorption of photons. Under illumination, the noise current spectral density due to recombination-generation process is given by [41]

$$\left\{ i_{g-r}^{2} \right\} = \frac{4qI_{ph}\left|M(\omega)\right|^{2}}{M_{0}} \tag{2.3}$$

where I_{ph} is the average photocurrent, M_0 is the DC photoconductive gain, and $M(\omega)$ is the dynamic photoconductive gain. The dynamic photoconductive gain is expressed as

$$M(\omega) = \frac{t_{n}}{t_{transit}} \bullet \frac{1}{(1 + jt_{n}\omega)} \tag{2.4}$$

and the DC photoconductive gain is expressed as

$$M_{0} = \frac{t_{n}}{t_{transit}} \tag{2.5}$$

so that Eq.(2.3) can be rewritten as

$$\left\{ i_{g-r}^{2} \right\} = \frac{4qI_{ph}M_{0}}{1 + t_{n}^{2}\omega^{2}} \qquad (2.6).$$

where t_n and $t_{transit}$ are the mean life time and the transit time of the electron, respectively. Assuming that the bandwidth is low ($BW \ll 1/t_n$), the mean squared generation-recombination noise current can be written as

$$\langle i_{g-r}^2 \rangle = 4qI_{ph}M_0BW \qquad (2.7).$$

Under a low bias, the re-injection of charge carriers in a MSM photodiode is blocked by the double Schottky barrier and thus the photoconductive gain of a MSM diode approaches unity. The generation-recombination noise of an MSM approaches twice the photocurrent shot noise at low frequency ($\omega << 1/t_n$).

Among the four noise contributions considered, the generation-recombination noise dominates the MSM photodiode array noise spectrum at the low frequency range ($f < 2\pi/t_n$). The photocurrent shot noise dominates at a high frequency range. The magnitude of the detector noise is in the order of 8 pA/√Hz allowing a SNR of 50 dB with a 1GHz bandwidth assuming a 500μW incident optical power.

2.1.2 Laser Diode

An optical source with a wavelength within the detector absorption spectrum is chosen to generate the optical carrier. The criteria for the optical source selection were studied thoroughly by M.Veilleux in his thesis [30]. He pointed out the requirements for the optical source are a high conversion efficiency to minimize the conversion loss, a high spatial coherence to maximize the coupling coefficient, and a high modulation bandwidth for broadband operation. A Mitsubishi ML6411C AlGaAs injection laser diode with a 50 μm core multimode fiber pigtail was chosen for M.Veilleux's application. This laser diode has a nominal wavelength of 780 nm and a quantum efficiency of about 0.4 W/A with 20 mW peak power. The device was tested with a 2.0 GHz modulation bandwidth and has two optical emission peaks with an output power of 5 mW total.

A multimode fiber pigtail was chosen over a monomode fiber because of its potentially high coupling efficiency; however, the pigtailing process used by manufacturer has a 50% coupling loss. The external quantum efficiency of the 10 lasers after pigtailing is 0.2 W/A on average. In this project, ML6411C laser diodes were used for optical sources because of their compatibility with existing components.

2.1.2.1 Laser noise

The noise of a Fabry Perot laser diode originates from two sources: shot noise and relative intensity noise (RIN). The laser shot noise is caused by the junction current of the laser and the relative intensity noise is caused by the amplified spontaneous emission inside the gain medium [44]. The noise performance of the ML6411C is specified in terms of a dynamic range which includes the contributions of both laser shot and RIN noises. The worst specified dynamic range values for ML6411C are 125 dB/Hz at 20kHz and 128 dB/Hz at 10 MHz [45]. These dynamic range values are functions of both optical power and optical feedback; these values are obtained under a strong radio frequency (RF) modulation (35mA$_{p\text{-}p}$) with a low (<0.1%) optical feedback. In the proposed optical system, the laser is expected to be operating under a high modulation index to maximize the SNR performance and a 1x10 optical splitter serves as a 10 dB attenuator to attenuate the reflected light. The dynamic range of the laser is expected to be near the 125 - 128 dB/Hz range.

2.1.3 Optical Components

A Northern Telecom 50 μm core multimode optical fiber with a numerical aperture of 0.2 is used for the optical system because of its high coupling efficiency. The fiber loss at 850 nm wavelength is specified to be 2.4 dB/km. For the application proposed, the fiber length is expected to be few meters and thus the fiber loss is insignificant compared to other losses. The two major sources of insertion loss are optical splitters and optical connectors. The optical splitter is a 1x10 biconical-taper fiber splitter from Canstar Optics. From the manufacturer's data, the excess loss of the 1x10 multimode optical splitter is less than 3 dB for all 10 splitters [46]. Two types of optical connectors used for interconnecting components are fiber connector (FC) and physical contact fiber connector (PC/FC). The insertion losses for the fiber connectors are expected to be less than 0.5 dB/splice. The overall optical loss from the laser to the MSM photodiode is expected to be less than 15 dB.

2.1.3.1 Optical Noise

When multimode fiber components are used, some other problems related to multimode propagation, such as modal dispersion and modal noise, must be considered. The modal dispersion limitation of multimode fiber (~500 MHz/km at 850nm) is insignificant because of the short fiber length of the proposed system. For a fiber length of few meters, the dispersion limited bandwidth is on the order of 100 GHz which is much greater than the electrical bandwidth.

Modal noise, also known as speckle noise, is caused by the random interference of different modes which propagate at slightly different velocities. The modal noise in this system arises primarily from the biconical splitter. If a mode selection process is present, when the distribution of power in the various modes changes, the power incident on the detector can change. The average power to variance ratio of a similar 1x8 biconical-taper splitter was reported at 28.5-33.0 dB with the input fiber under a constant vibration to enhance the fluctuation level [47]. The modal noise is expected to be lower with no vibration. The SNR of the fiber system is expected to be about 30 dB.

2.1.4 Receiver Amplifier

The required amplifier gain for compensating the total path loss from optoelectronic conversions and optical propagation losses is determined to be approximately 60 dB[4]. A low noise 50 Ω gain block amplifier design with a gain of approximately 60 dB was considered for this application. A prototype of the amplifier was built and measured to have a gain of 60 dB with an output noise floor range of -106 dBm/Hz and with a bandwidth of 1.5 GHz.

The dynamic range of the amplifier is determined by its maximum available output signal and its noise floor. The maximum output power of the receiver amplifier is limited by the maximum electrical input of the transmitter which corresponds to 10 dBm for a 100% modulation index. The maximum dynamic range of the receiver amplifier with the low noise 50 Ω amplifier design is estimated to be 116 dB/Hz.

2.1.5 Estimated System Performance

Based on the available components, the system parameters, such as the bandwidth, the dynamic range, and the isolation can be estimated. The dynamic range of the system is expected to be dominated by the amplifier thermal noise and is expected to be about 116 dB/Hz. The bandwidth of the system is limited by the receiver amplifier and is expected to be 1.5 GHz. The isolation of the crosspoints is determined by the MSM photodiode array which is expected to be about 40-50 dB over the 1.5 GHz bandwidth.

2.2 Applications under Consideration

Based on the component performances described above, we can estimate the performance of the processor in different applications such as cascadable switch matrix and reconfigurable filter.

2.2.1 Cascadable Switch Matrix

By cascading a number of switching matrices, one can realize a larger switching network with a smaller number of crosspoints than a single large matrix implementation. For example, a 3 level Clos network, shown in Figure 2.6, is one such non-blocking network. A direct 100x100 non-blocking switch matrix requires 10000 crosspoints; a 3 level Clos network can implement the same matrix with only 3000 cross points. The size of an optoelectronic switch matrix is limited by two factors: the cumulative capacitance of the detector array and the available optical power [36]. By subdividing large matrices into smaller matrices, one can reduce the cumulative capacitance on each detector array and the required optical power from each source and thus extend the size limit of a matrix [48]. However, this type of network requires multiple optoelectronic and electo-optic conversions through the switching matrices, and these multiple conversions can induce additional signal degradation from various sources, such as noise accumulation, bandwidth reduction, and crosspoint isolation.

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[4] see Appendix A for detailed calculations.

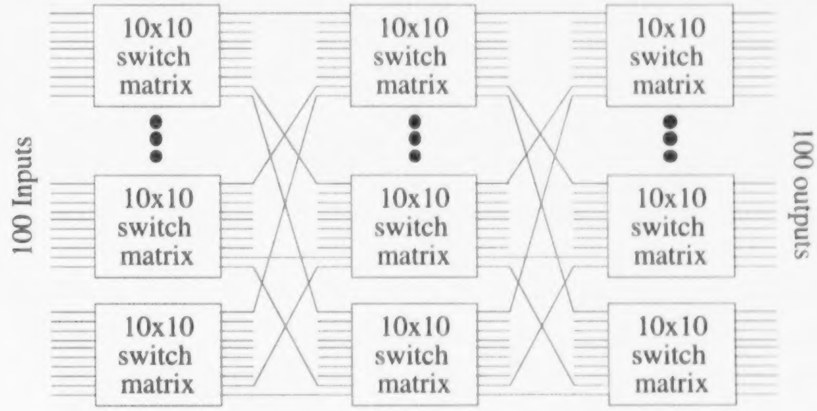

100 Inputs
10x10 switch matrix
10x10 switch matrix
10x10 switch matrix
10x10 switch matrix
10x10 switch matrix
10x10 switch matrix
10x10 switch matrix
10x10 switch matrix
10x10 switch matrix
100 outputs

Figure 2.6 A 100x100 3 layer Clos network

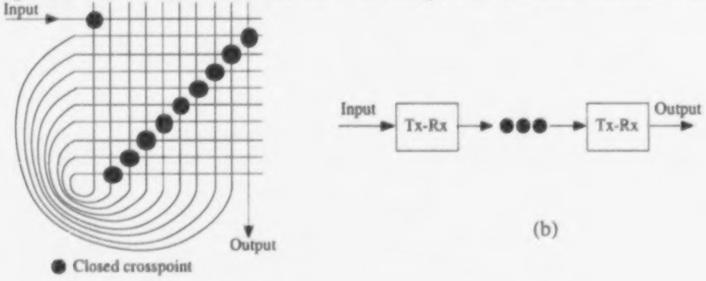
In Appendix B, the effects of these impairments were studied. Based on a first order low pass model, the bandwidth of a multistage network decreases with a factor of $\frac{f_c}{\sqrt{\sqrt[N]{2}-1}}$ where N is the number of stages and f_c is the 3 dB frequency of each identical stage. In Appendix B, the effects of noise accumulation and bandwidth was also studied under three different conditions. With an ideal square box low pass response model, the signal to noise ratio (SNR) decreases at a rate of 1/N as N is the number of cascading stages. With a first order response model, the SNR decreases at a rate slower than 1/N; however, the bandwidth of such system would decrease by a factor of $\frac{f_c}{\sqrt{\sqrt[N]{2}-1}}$. In the third case, the bandwidth of individual stage is expanded to compensate the bandwidth reduction. The resulting SNR degrades at a rate much faster than 1/N.

The crosstalk from non-ideal crosspoints in a multistage switch network is found to be better than the single stage network of the same dimension because of a reduction in the number of adjacent "OFF" crosspoints. The exact value of the improvement is related to the network topology used.

Nonlinearity is another degradation of a multistage network. In a broadband system, nonlinearities can generate harmonic distortion and intermodulation products which may lead to cross channel interference. When this distortion couples with multiple nonlinear stages, the intermodulation among the signals and their harmonics shifts the interference in both spectral directions. A common approach to estimate cross-channel interference is to tabulate all intermodulation products within an allotted frequency channel by tracking every signal and its harmonics [11].

The proposed system is not expected to be highly linear because the components used are optimized for bandwidth but not for linearity, especially the laser diode and the receiver amplifier. This linearity problem can be simply overcome by replacing the devices with highly linear devices; however, the current cost of such devices is high (a highly linear laser diode used for optical analog transmission by Fujitsu was priced over \$10,000). The effects of non-linearity can be managed by using narrow band measurement techniques and applying a low level signals to avoid distortions.

One possible application for the signal processor matrix is to study the behavior of cascaded switching matrices by recirculating a signal through multiple passes in one matrix. Figure 2.7 shows the proposed configuration which connects inputs and outputs of the system to form a series of transmitter and receiver pairs. Then the noise behavior and spectral impairments can be measured and compared with theoretical models.



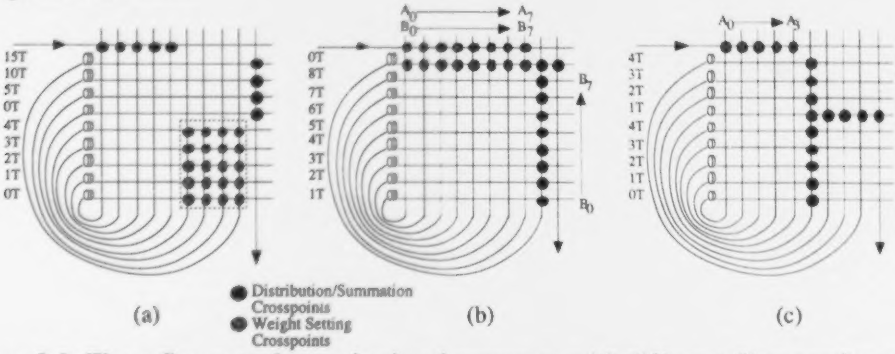
(a)

(b)

Figure 2.7 The proposed processor configured as a serial of Tx-Rx pairs. (a) the configuration diagram and (b) a block diagram.

2.2.2 Reconfigurable Discrete Time Filter

The reconfigurable discrete time filter is the chief application considered for this processor. With the replaceable optical delay lines and adjustable tap weights, the proposed system is well suited for testing various FIR and IIR filter configurations. Figure 2.8 shows the optoelectronic signal processor configured as three different types of discrete time filter. With electronically controlled filter tap coefficients, these filters are potentially suitable for adaptive filtering applications such as adaptive equalization and optimal detection.



(a) (b) (c)

Figure 2.8 The reflex optoelectronic signal processor with different filter configurations. (a) a 20 tap FIR filter. (b) Direct Form I IIR filter, and (c) Direct Form II IIR filter. Note that the gray circle represents a crosspoint with a continuous variable weight from -1 to +1 and the black circle represents a crosspoint with a constant weight of 1.

Besides the usual requirements on noise, bandwidth and linearity, other additional factors must be considered for the filter applications. First, the round-off or truncation of the system parameters can deviate the response of the filter from the desired values. Two major sources of the round-off errors are the filter tap coefficient settings and the delay time inaccuracies.

The optoelectronic weight setting process has a finite precision which leads to a round-off error on filter coefficients. These errors can move the poles and zeros of the filter in the complex frequency plane. Depending on the sensitivity of the pole and zero, this shift can cause the system response to deviate from the designed response; in the case of IIR filters, this deviation might even lead to instability.

The second inaccuracy arises because the electrical responses of the parallel stages can introduce differential magnitude and phase differences. In the following sections, the sensitivities of the filter response to these errors will be studied and their degradation effects will be estimated based on the component parameters.

2.2.2.1 Sensitivity analysis of round-off error on system parameters

To account for perturbations of time delay and filter coefficient, we rewrite Eq 1.1 as

$$\hat{h}(t)=\sum_{n=-\infty}^{\infty}(a_n+\delta a_n)\delta\big(t-(nT_s+\delta T_n)\big) \qquad (2.8)$$

where δa_n is the truncation error of the filter coefficient, and δT_n is the round-off error of the delay time. These errors are modeled as two uniformly distributed random variables.

2.2.2.2 FIR Tap Weight Sensitivity

Following the approach employed in Ref.[7], the round-off effect on the filter weights can be represented as an additional term in each weight. The new weight can be expressed as

$$\hat{a}_n = a_n + \delta a_n \tag{2.9}$$

and Eq.(1.1) for an FIR response can be rewritten as

$$\hat{h}(t) = \sum_{n=0}^{M} \hat{a}_n \delta(t - nT) \tag{2.10}$$

Substitute Eq.(2.9) into Eq.(2.10) and separate the ideal terms and variation terms

$$\hat{h}(t) = \sum_{n=0}^{M} a_n \delta(t - nT_s) + \sum_{n=0}^{M} \delta a_n \delta(t - nT_s) \tag{2.11}$$

Then the frequency response of the round-off filter is determined by taking the Fourier transform of Eq.2.11

$$\hat{H}(f) = H(f) + \Delta H(f) \tag{2.12}$$

where

$$\Delta H(f) = \sum_{n=0}^{M} \delta a_n e^{j2\pi fnT_s}. \tag{2.13}$$

Then the error on the response due to the round-off on filter coefficients can be estimated by:

$$\left|\Delta H(f)\right| = \left|\sum_{n=0}^{M} \delta a_n e^{j2\pi fnT_s}\right| \le \sum_{n=0}^{M} \left|\delta a_n\right| \left|e^{j2\pi fnT_s}\right| \tag{2.14}$$

and $\left|e^{je^{j2\pi fnT_s}}\right| = 1$. Eq(2.14) can be rewritten as

$$\left|\Delta H(f)\right| \le \sum_{n=0}^{M} \left|\delta a_n\right| \tag{2.15}$$

The optoelectronic weight is set by adjusting the bias voltage of a photodetector; therefore, the accuracy of the output weight is directly related to the bias resolution. Assuming the relation between voltage and photoresponse is linear , the effect of weight uncertainty can be estimated by evaluating the accuracy of the bias source. Actual nonlinearity of the bias and responsivity relationship can be counteracted by previous calibration, if the bias is controlled by a voltage source with B bits resolution, then the upper bound uncertainty of a FIR filter response with M taps can be expressed as

$$|\Delta H(f)| \le K_R 2^{-B} M \tag{2.16}$$

where K_R is a proportionality constant between bias voltage and output voltage, B is the bias range of the MSM photodiode, and M is the number of taps. The bias saturation effect in the MSM response can be accounted for by replacing B with a smaller effective resolution B_{eff}. From Eq.(2.16), the error on the FIR filter response is strictly a function of the filter length and the bias resolution. Figure 2.9 illustrates the response of a 20 tap bandpass FIR filter with a 10 bit effective resolution weight coefficient. The round-off effect is insignificant in the passband response but does degrade the stopband performance.

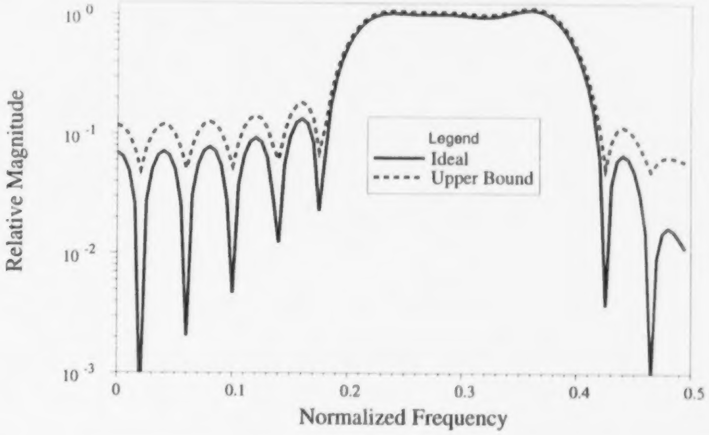


Figure 2.9 The response of 20 tap bandpass FIR filter with the 10 bit resolution.

From the above analysis, the effect of the noise imposed on the bias voltage can be estimated by replacing the round-off voltage with the variance of the noise voltage and the upper bound of the noise power is given

$$|N_{FIR}| \le K_R^2 \delta_b^2 M \tag{2.17}$$

where δ_b^2 is the noise power superimposed on the bias line.

2.2.2.3 IIR Tap Weight Sensitivity

In an IIR filter, the weight inaccuracy has two effects on the filter response. First, random time varying fluctuation of the bias causes an additive noise on the output spectrum. In the case of optoelectronic weight setting, the round-off noise is due to the noise voltage imposed upon the bias voltage modulating the responsivity. Second, a constant offset due to inaccuracy of the tap weights is randomly distributed in a range of values but is constant over time. This offset can force the poles-zeros of the filter to move from their ideal positions and can lead to instability in some IIR filter designs.

The effect of the round-off noise can be calculated by following the approach used in Ref.[49]. In this approach, the round-off noise power is modeled as an additive noise with a mean of zero and a variance of δ_{tap}. First, the round-off noise sources are transformed to the input side. Then the IIR section is replaced with an equivalent impulse train, $h_{ef}(nT)$. The equivalent noise power of the pure feedback IIR filter section is given by

$$N_{IIR}^2 = (N+1)\left(\sum_{n=-\infty}^{\infty}\left|h_{ef}(nT_s)\right|^2\right)\delta_{tap}^2 \tag{2.18}$$

where $h_{ef}(nT)$ is the impulse response of the IIR section, N is the number of IIR delays, and δ_{tap} is the noise variance of the tap weight fluctuation. For a Direct form I IIR filter, the upper bound round-off noise power is given by

$$N_{DF\,I}^2 = (M+N+1)\left(\sum_{n=-\infty}^{\infty}\left|h_{ef}(nT_s)\right|^2\right)\delta_{tap}^2 \tag{2.19}$$

where M is the number of FIR delay stages. The upper bound round-off noise power for a Direct form II IIR filter is given by

$$N_{DF\,II}^2 = \left(N\sum_{n=-\infty}^{\infty}\left|h_{ef}(nT_s)\right|^2 + M + 1\right)\delta_{tap}^2 \tag{2.20}.$$

In the proposed processor, the round-off noise from the time variation of tap weights is expected to be insignificant and can be controlled by filtering the biasing voltage. From previous analysis, the processor noise is dominated by thermal noise of the receiver amplifier. Since a receiver amplifier is associated with each summing node rather than each delay, Eq. (2.18) needs to rewritten as

$$N_{IIR}^2 = \left[L\left(\sum_{n=-\infty}^{\infty}\left|h_{ef}(nT_s)\right|^2\right)+1\right]\delta_{th}^2 \tag{2.21}$$

where L is the number summing nodes in the IIR section and δ_{th}^2 is the receiver thermal noise from each receiver amplifier. The extra 1 in Eq.2.21 represents the noise contribution of the the final optolectronic conversion in the IIR section. The effect of receiver noise can be determined by modifying Eq. (2.18) and (2.19) as

$$N_{DF\,I}^2 = \left[(K+L)\left(\sum_{n=-\infty}^{\infty}\left|h_{ef}(nT_s)\right|^2\right)+1\right]\delta_{th}^2 \tag{2.22}$$

and

$$N_{DF\,II}^2 = \left(L\sum_{n=-\infty}^{\infty}\left|h_{ef}(nT_s)^2\right| + K + 1\right)\delta_{th}^2 \tag{2.23}$$

where L and K are the numbers of summation nodes in IIR and FIR sections respectively.

The round-off offset, which is the constant portion of the round-off error, can couple with the round-off noise to cause a severe degradation on the filter. The effect of this offset can be estimated by calculating the sensitivity of the filter response to tap weight variation.

From the previous discussion, a general IIR filter consists of both a FIR section and a pure IIR section. Since the effect of round-off offset on FIR section has been discussed in the last section, the following discussion will only focus on the pure IIR section (i.e. all a_n's are set to zero).

The coefficients, b_n, deviate from their ideal values by a given amount δb_n, and the new coefficients are given as

$$\hat{b}_n = b_n + \delta b_n \ . \tag{2.24}$$

Substituting Eq. (2.24) into Eq. (1.5), the new transfer function can be expressed as

$$\hat{H}(f) = \frac{1}{1 - \sum_{n=0}^{N} \hat{b}_n e^{-j2\pi f n T_s}} \tag{2.25}$$

The original filter response H(f) is assumed to be stable so that Eq. (2.25) can be expanded into a Taylor series. With a first order approximation, the deviation of the frequency response due to round-off error can be determined by differentiating Eq.(2.25) with respect to each coefficient

$$S_{H(f)}^{b_n} \cong \frac{\partial H(f)}{\partial b_n} \cdot \delta b_n \tag{2.26}$$.

Substituting Eq.(2.25) into Eq.(2.26), Eq.(2.26) is rewritten as

$$S_{H(f)}^{b_n} \cong H^2(f) \cdot e^{-j2\pi f n T_s} \cdot \delta b_n \tag{2.27}$$.

Based on Eq. (2.27), an upper bound of the error on the frequency response due to round-off can be expressed as

$$\begin{aligned} \left|\Delta H(f)\right| &\le \textstyle\sum_{n=1}^{N} \left|S_{H(f)}^{\delta b_n}\right| \\ &\le \textstyle\sum_{n=1}^{N} \left|H^2(f) \cdot \delta b_n\right| \end{aligned} \tag{2.28}$$

If the round-off error is limited to one bit resolution, 2^{-B},. then Eq. (2.28) can be rewritten as

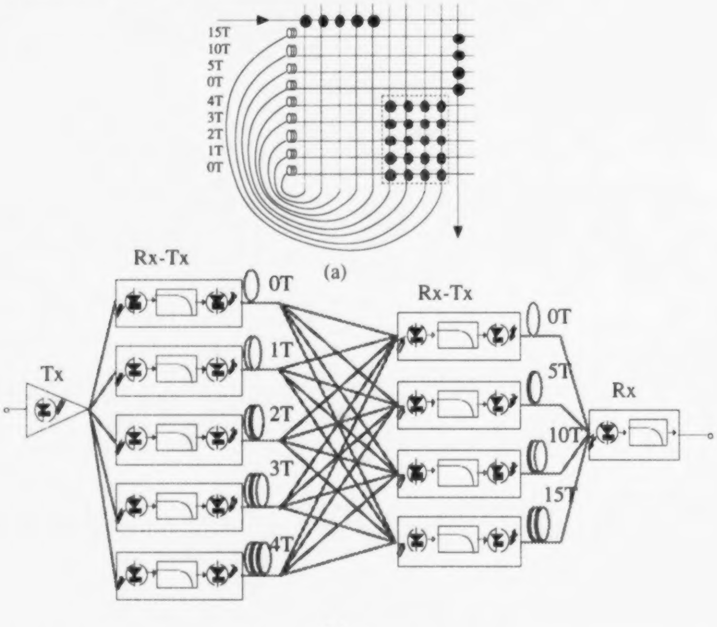
$$\left|\Delta H(f)\right| \le 2^{-B} N \left|H^2(f)\right| \tag{2.29}$$.

From Eq.(2.29), the effect of the round-off offset is strongly dependent on the square of the bandpass gain and can be minimized by limiting the bandpass gain to near to unity.

2.2.2.4 Time delay sensitivity analysis

The accuracy of optical time delays used in this discrete time signal processor is limited by the fabrication process of the optical fiber delay lines. The fiber delay lines used in this project were assembled manually and the overall accuracy is limited to approximately one inch which corresponds to a delay inaccuracy of 1/10 ns. This inaccuracy may introduce a sufficient phase difference at high frequency to cause a major distortion on the filter response.

A variety of simulation techniques are used to study the impact of delay line inaccuracy on the response[8, 13, 49, 50]. For a general study, a simple simulation model consisting of a delay with a uniformly distributed random delay error was used to gauge the effect of delay variation on a bandpass (f_p=0.2-0.4) FIR filter. A FIR model is chosen for this simulation over an IIR model because the FIR filter, in general, exhibits fewer design specific characteristics than an IIR filter.

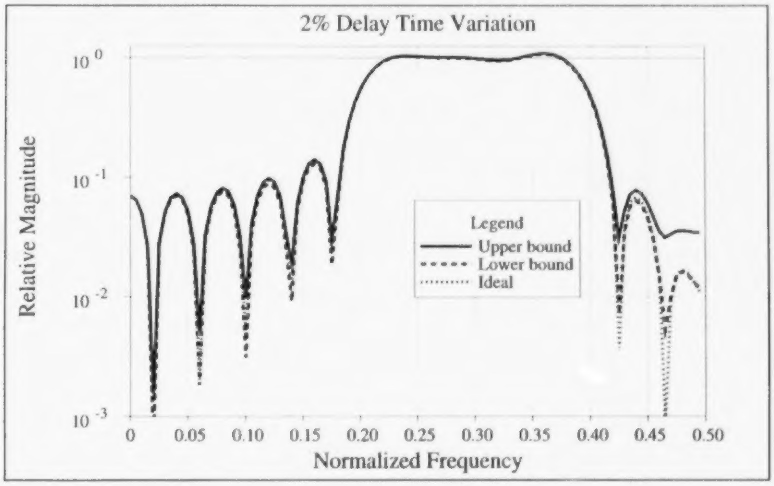


(b)

Figure 2.10 The 20 tap FIR filter simulation model. (a) A conceptual diagram of the filter. (b) A block diagram of the filter

The filter model illustrated in Figure 2.10 is based on a reflex 20 tap FIR design with a 10x10 switch matrix. The simulation program is listed in Appendix C.

Figure 2.11 shows the simulation results from the model under different delay variations from 2% to 20% of a normalized time unit[5]. The responses exhibit a strong dependence on the time accuracy. With a 2% delay variation, the effect of the delay inaccuracy is minimal which is consistent with the simulation results in Ref.[13]. With a 20% delay variation, the filter performance is severely degraded at the stopbands, especially the upper stop band. At the expected accuracy of the optical delay lines which is about 10% delay variation, a +/-1% variation on the passband response was observed from the simulation results; however, the upper stopband performance is degraded by a factor of 5 dB.



(a)

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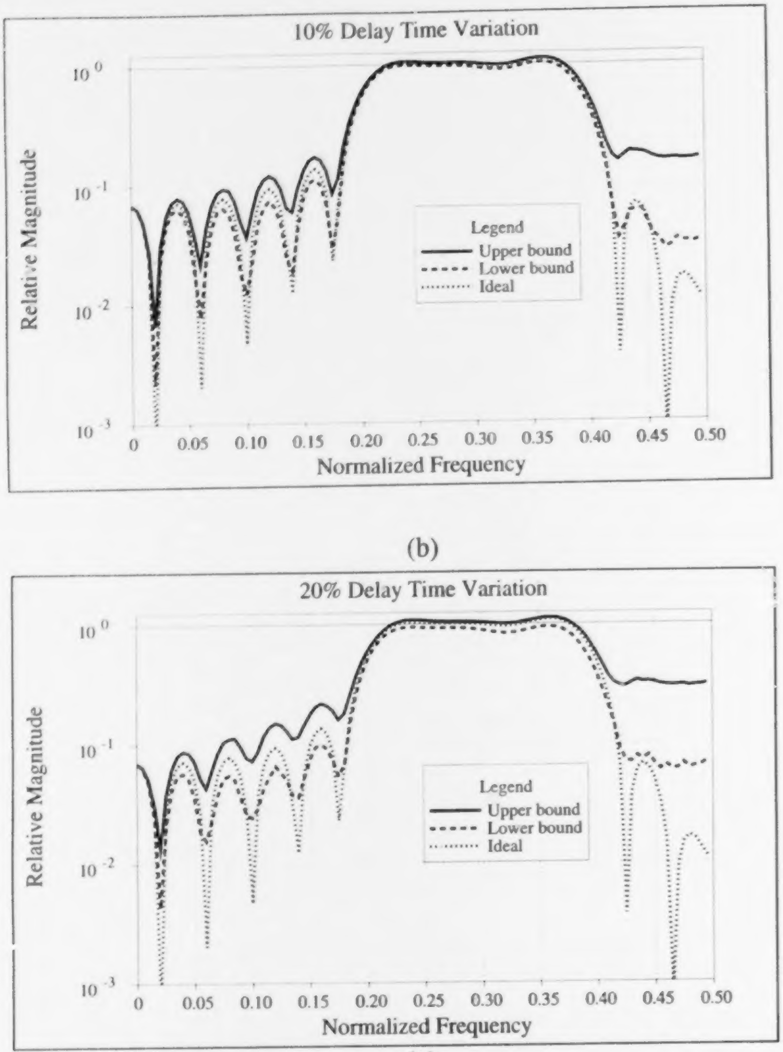
[5] A normalized time unit is normalized against one incremental delay used and normalized frequency is normalized against the sampling frequency.



(c)

Figure 2.11 The effects of the delay variation on a bandpass FIR filter. (a) 2%, (b) 10%, and (c) 20% variations.

2.2.2.5 Electrical Response Sensitivity Analysis

Due to the unique reflex structure of this processor, the input signals are fed through a number of different optical and electrical paths and then combined to form the overall output. The frequency response differences of these paths can cause additional phase and amplitude distortions which degrade the overall response. The optical paths are relatively insensitive to frequency and broadband with respect to the electrical paths and the optical paths are too short for any significant dispersion effect; therefore, the optical paths can be assumed to have a constant frequency response. On the contrary, the electrical path has a relatively narrow bandwidth which limits the system response.

Response variations in the signal paths can produce noticeable distortions on the overall response. A frequency sensitive coefficient is used to account for this frequency dependency of the electrical paths. With this model, Eq.(1.2) can be written as

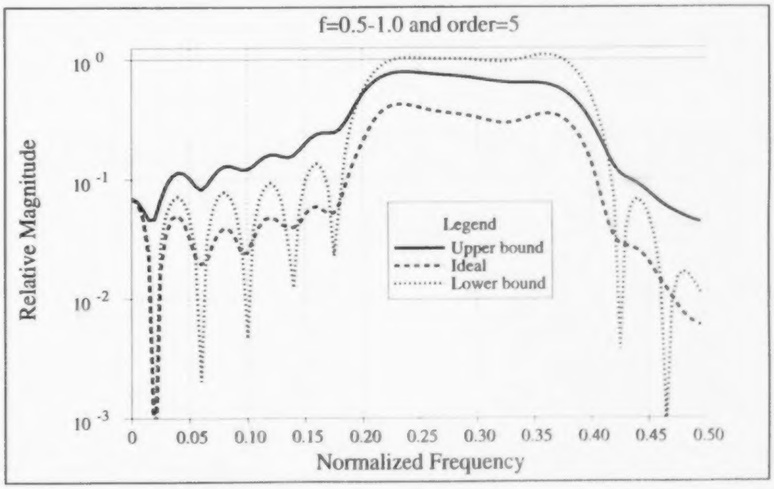
$$H(f) = \sum_{n=0}^{M} a_n(f) e^{-j2\pi n T_s f} \tag{2.30}$$

and

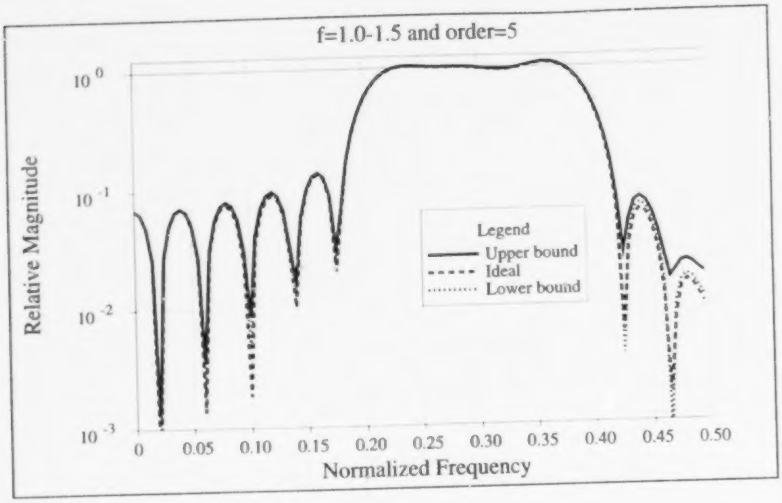
$$a_n(f) = a_n \cdot H_n(f) \tag{2.31}$$

where $H_n(f)$ is the frequency response related to each coefficient. If all $H_n(f)$ are identical, their effect can be simply accounted for as an additional series transfer function imposed on the overall response. If the transfer functions are significantly different from each other, then these differences in both phase and magnitude can lead to an incoherent addition at the output. To obtain an analytical estimation of this distortion would require detailed statistical information on the electrical frequency response of each path which is difficult to obtain.

To account for the frequency response variation of a Tx-Rx pair, a lumped parameter model, consisting of a multiple first order response with pole locations randomly distributed throughout a given frequency range, is used to model the Tx-Rx pair response. A Monte Carlo simulation approach based on this lumped parameter model and the same bandpass filter design, shown in Figure 2.10, is employed to simulate the response variation. Figure 2.12 shows three different cases with different frequency ranges and different filter orders.



(a)



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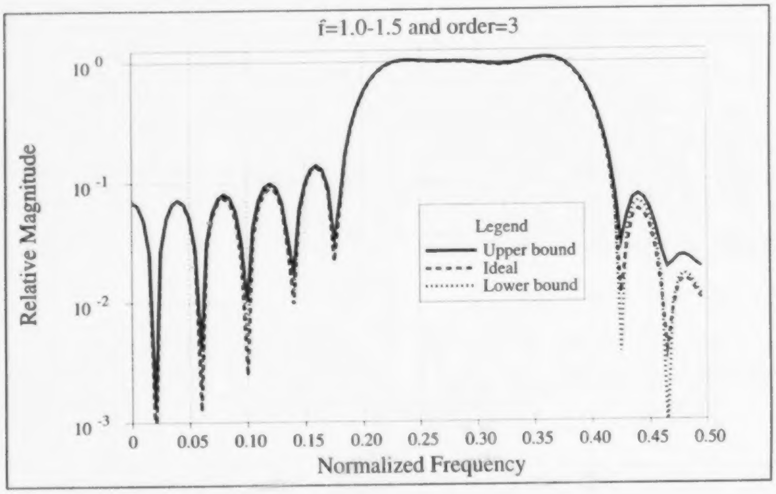


(c)

Figure 2.12 The effects of the electrical responses on a reflex bandpass filter. (a) f=0.5-1.0 and order = 5, (b) f=1.0-1.5 and order =5, and (c) f=1.0-1.5 and order=3. f is the 3 dB frequency of a Tx-Rx pair.

Figure 2.12.a shows that the effect of the signal path is not significant provided the 3 dB frequency response is greater than one normalized frequency unit. For example, if the signal processor is designed for a 500 MHz programmable bandwidth, a 3 dB corner frequency greater than 1 GHz must be maintained to minimize the effect of the electrical system on the overall response.

3.0 TRANSMITTER MODULE

The purpose of the transmitter module is to provide stable bias current and cooling to the 10 optical sources that perform the optoelectronic conversion of the input electrical signal. The optical power distribution and time delay necessary for each laser output are housed in each transmitter card. In this chapter, the functions and detailed structures of the transmitter module will be described and measured results will be presented.

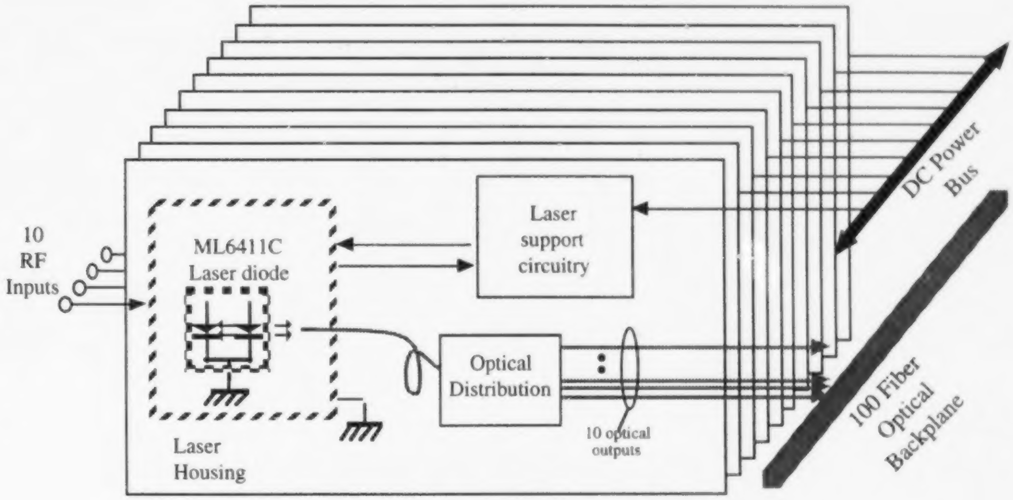


Figure 3.1 Block diagram of the transmitter module

Figure 3.1 shows a block diagram of the transmitter module. The overall transmitter module is organized into 10 transmitter cards; each card houses one laser diode and its supporting circuitry. These cards are mounted in a standard 3U 84HP card cage with a card length of 220 mm. The cards are supplied with a 5 volt, 20 ampere DC power bus. The 100 outputs of the transmitters are connected to an optical backplane composed of 100 FC/PC optical connectors. Figure 3.2 is a picture of the optical back plane.

3.1 Transmitter Card

On each transmitter card, a laser diode with its biasing and thermal regulation circuitry functions as a stable optical source to be modulated with an external radio frequency (RF) input. The modulation is achieved by injecting the RF signal into the diode current with a biasing insertion circuit. The outputs from each laser are split identically ten ways by means of commercially available multimode biconicial taper power splitters to illuminate 10 1x10 photodiode arrays. An additional section of optical fiber is inserted in the optical path between the laser and the power splitter to provide the time delay for signal processing. These delay lines are replaceable and each delay line is connectorized with FC connectors and is housed inside an aluminum box with two FC mating sleeves for external connection.

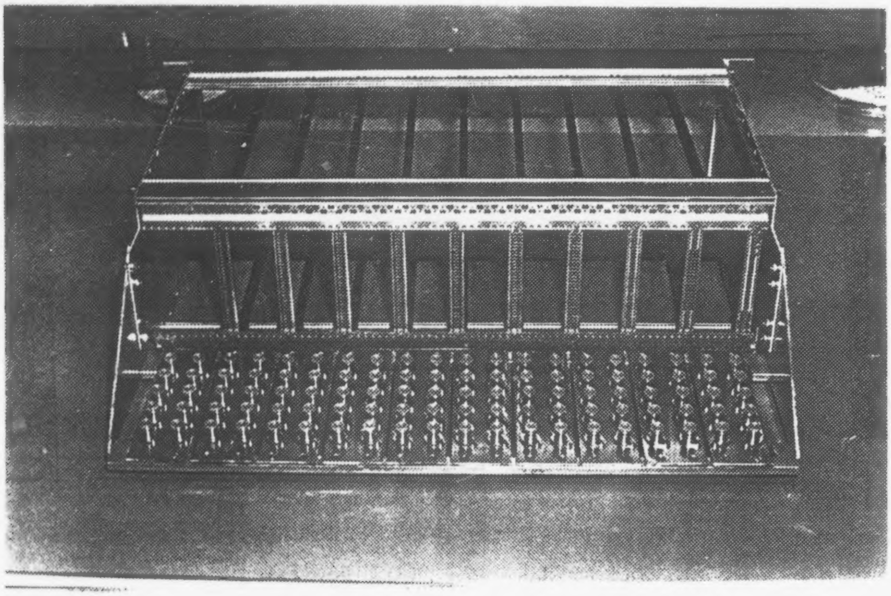


Figure 3.2 A picture of the optical backplane.

Each transmitter card performs four major tasks: laser support, laser housing, optical delay, and optical distribution. The laser support circuitry supplies the necessary bias and thermal regulation for the proper operation of the laser diode. The laser housing provides the required mechanical support, thermal coupling, and electromagnetic decoupling for the laser diode. The laser housing contains the RF insertion unit which matches the low impedance laser to a 50 ohm external modulation source. The optical distribution and the optical delay performs the optical side of the optoelectronic signal processing consisting of the power splitting and time delay.

3.1.1 Laser Support Circuitry

For a laser diode to be modulated with a broadband signal, certain biasing conditions must be met. First, the diode must be biased above the lasing threshold for fast response [44]. An optical power regulation circuit is added to stabilize the average optical output from the laser. The regulator also stabilizes the output power against the long term drift of the laser output due to aging or other environmental effects [51].

The laser circuit described in the following sections are a modified version of laser transmitter designed by David Clegg of TRLabs.

3.1.1.1 Laser Power Regulation Circuit

Besides the threshold requirement, two features are added to the power regulator to prolong the life of the laser. First, the manufacturer of the laser diode recommends the laser current should be gradually increased during the initial power on transition to prevent any damaging current surges [45]. Second, a normally closed switch is added across the laser diode to protect against static discharge when the laser is not in use. A power-up sequencing circuit is added to coordinate the execution of these operations.

Figure 3.3 is a schematic diagram of the laser power regulation circuit and the detailed circuit is listed in Appendix D. The circuit consists of two sections: power regulation loop and start-up sequencer. The power regulation loop also provides a soft start function and over-current protection as well as optical power regulation.

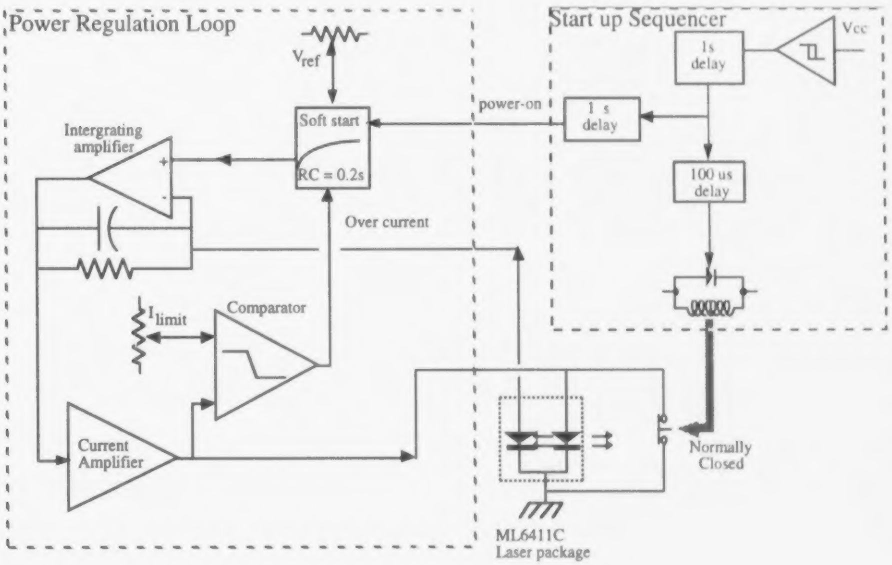
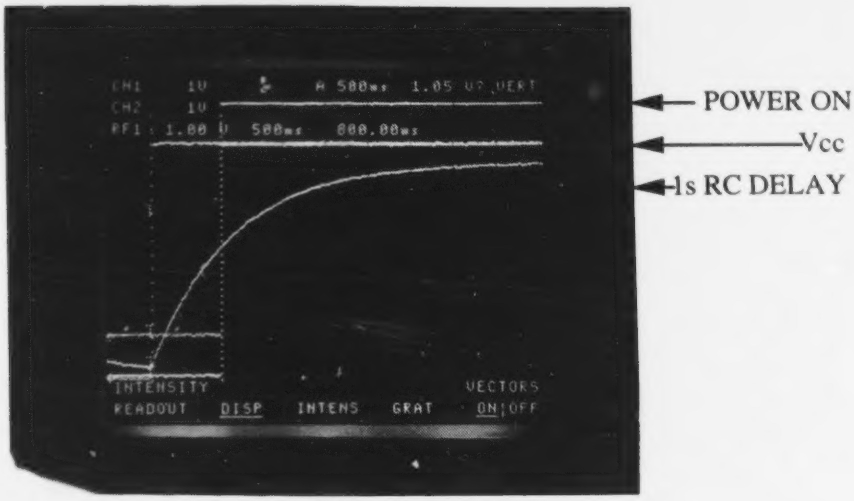

Power Regulation Loop
V_{ref}
Soft start
RC = 0.2s
Intergrating amplifier
+
-
Over current
I_{limit}
Comparator
Current Amplifier
power-on
Start up Sequencer
1s delay
Vcc
1 s delay
100 us delay
Normally Closed
ML6411C Laser package

Figure 3.3 A schematic diagram of the laser power regulator

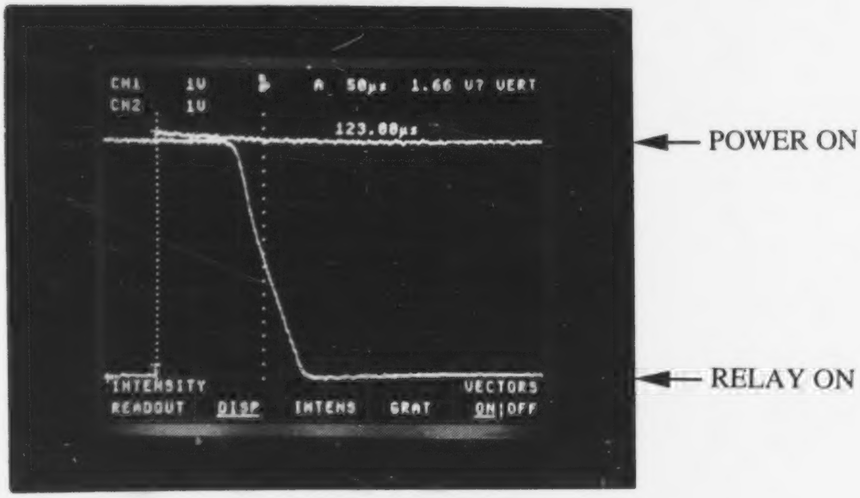
The start-up sequencer coordinates the operations of the card. First, the sequencer detects the supply voltage reaching a specific level (~0.5 V_{CC}) and then waits for an additional one second for the voltage to stabilize. After another 100 μs, it energizes a relay to release the static protection switch for the laser diode. One second after the supply voltage is stabilized, a power-up signal is sent to the power regulation loop to initialize the soft start circuit. Inside the soft start circuit, a long time constant RC (T~220 ms) circuit is used to charge up the reference input gradually to the preset value after the start-up signal is received.

The main part of the power regulation loop is a proportional and integrating (PI) control loop with a time constant of about 0.2 seconds. The optical power of the laser is sensed by monitoring the photocurrent from the back facet monitor diode mounted inside the laser package. This current is compared against a constant reference voltage and the difference between the photocurrent and reference voltage is amplified by an integrating amplifier with a time constant of about 0.2 seconds. This time constant is chosen to be four orders of magnitude longer than the time constant of the lowest RF input frequency (300kHz). This long time constant prevents the RF modulation signal from coupling into the power regulation loop. Such coupling could cause an additional instability in the feedback loop. The output from the integrating amplifier is then converted by a current amplifier into a current to drive the laser diode. A comparator monitors the laser diode current to prevent any excessive drive current. When the diode current is above a preset current level, I_{limit}, an over-current signal is sent to the soft start circuit to reduce the reference voltage and thus reduces the drive current. As a result of this additional feedback, the laser drive current is limited to below I_{limit} protecting the laser against damaging high drive current. Because of the slow response of the power regulation loop, this circuit will not protect the diode against an excessive RF drive signal (greater than 14 dBm).

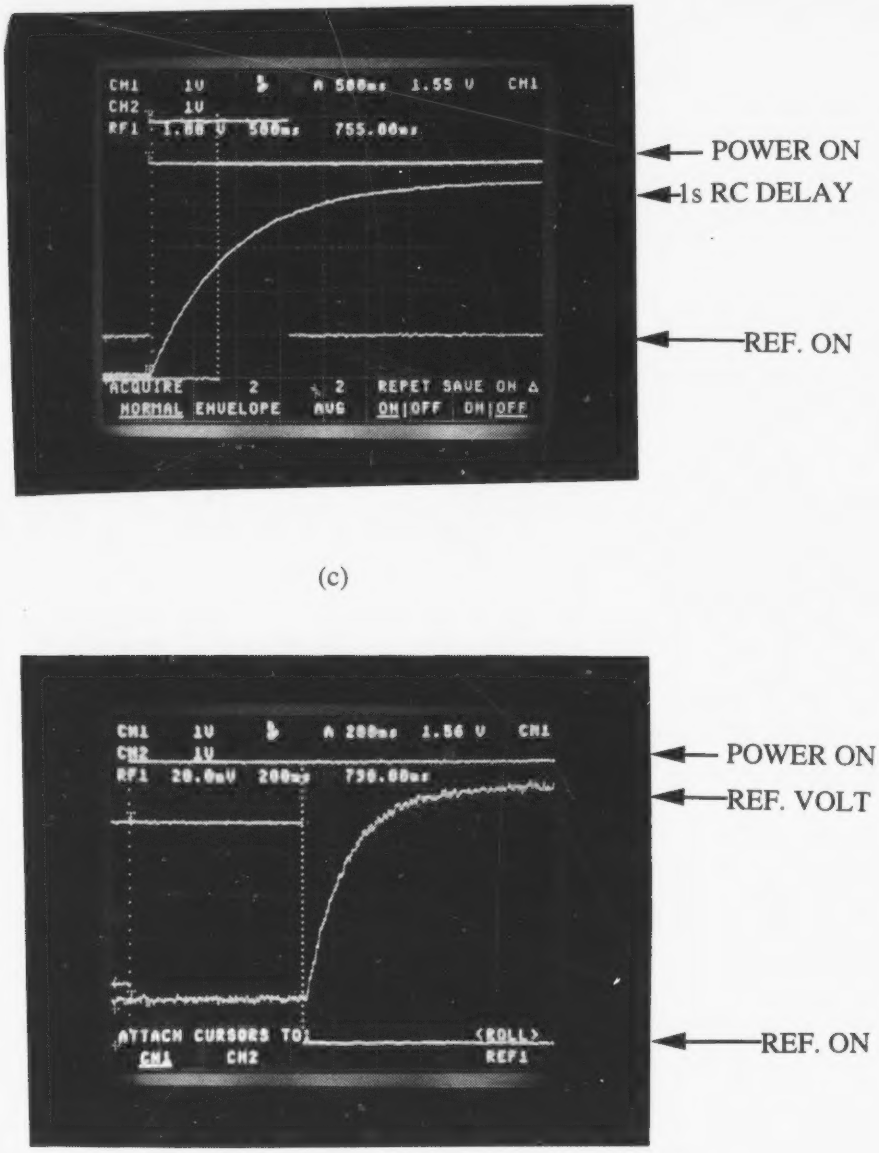
The start-up signal sequence at different points of the power regulation loop is shown in Figure 3.4. Figure 3.5 shows the optical output as a function of time. The initial ramping of the optical power lasts for a half second and then it requires 7.5 seconds for thermal regulation to settle to a steady state. From Figure 3.5, the variation of the optical output was measured to be less than 0.4 % (~20 μW for a 5mW output).


CH1 1V A 500ms 1.05 V? VERT
CH2 1V
RF1 1.00 V 500ms 800.00ms
INTENSITY VECTORS
READOUT DISP INTENS GRAT ON|OFF
POWER ON
Vcc
1s RC DELAY

(a)


CH1 1V A 50µs 1.66 V? VERT
CH2 1V
123.00µs
INTENSITY VECTORS
READOUT DISP INTENS GRAT ON|OFF
POWER ON
RELAY ON

(b)



(c)

(d)

Figure 3.4 The start-up sequence of the optical power regulation loop.
(a) the power supply voltage (Vcc), 1s delay RC charging curve, and the power-on signal.
(b) the power-on signal, and the relay voltage.
(c) the power-on signal, 1s delay RC charging curve, and the reference drive signal.
(d) the power-on signal, the reference drive signal, and slow rising reference voltage.

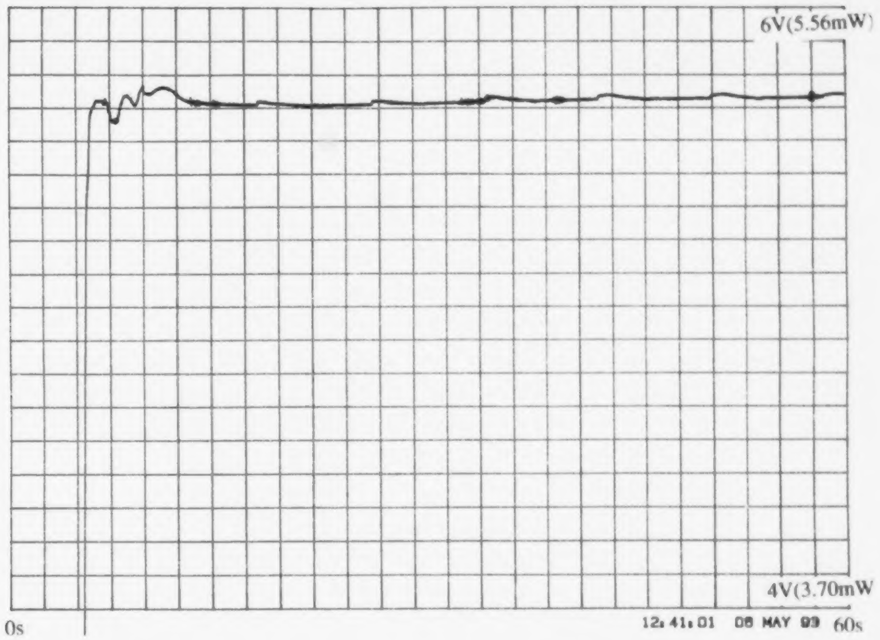


Figure 3.5 The initial transient of a transmitter card optical output.

3.1.1.2 Thermal Regulation Circuit

The junction temperature of the laser diode is another factor that affects the performance of a laser diode, especially its lasing threshold [52]. In general, the threshold current level of a semiconductor laser increases with the junction temperature. For an injection laser, such as ML6411C, the threshold current is exponentially related to the junction temperature and is expressed as [52]

$$I_{th} = I_o e^{-T/T_o} \tag{3.1}$$

where I_o is a proportionality constant and T_o is the characteristic temperature of the laser diode. The quantum efficiency of the laser is also dependent on the junction temperature [52]. To minimize these temperature effects on the lasers, a temperature regulation circuit is introduced to ensure that the laser is operated within a fixed temperature range.

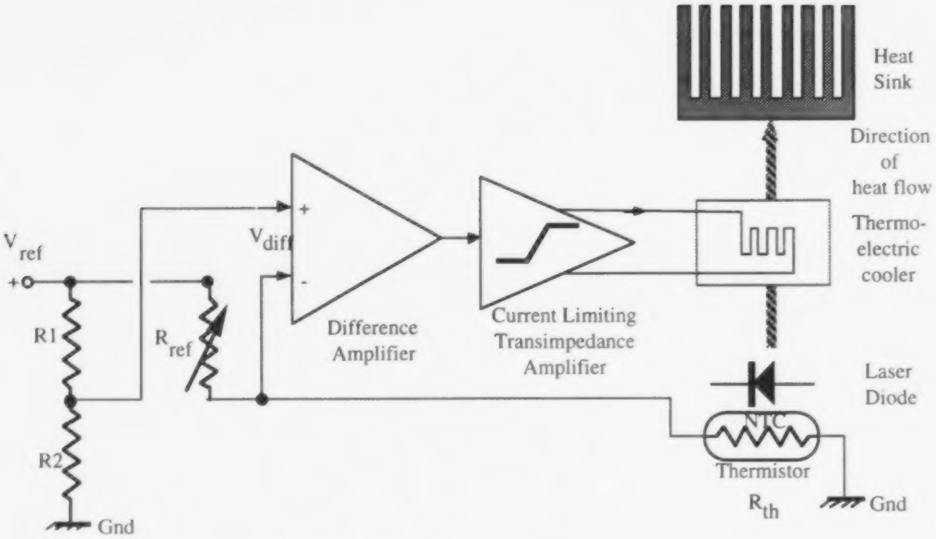

Heat
Sink
Direction
of
heat flow
Thermo-
electric
cooler
V ref
+
R1
R2
Gnd
R ref
V diff
+
-
Difference
Amplifier
Current Limiting
Transimpedance
Amplifier
Laser
Diode
NTC
Thermistor
R th
Gnd

Figure 3.6 A schematic diagram of the laser cooling circuit

Figure 3.6 is a block diagram of the thermal regulation circuit. The laser casing temperature is sensed by a thermistor which is adhered to the laser mounting bracket close to the laser package. This thermistor is connected with three other resistors to form an impedance bridge. One arm of the bridge, an adjustable resistor, sets the reference resistance value; the opposite arm is connected to the thermistor. The difference in voltage between the two arms is used to gauge the temperature. This voltage difference is given by

$$V_{diff} = V_{ref}\left[\frac{R_2}{R_1 + R_2} - \frac{R_{th}}{R_{ref} + R_{th}}\right] \tag{3.2}$$

where R_{ref} is the reference resistance of the measurement arm, R_1 and R_2 are the resistances for the fixed reference arms, and R_{th} is the resistance of the thermistor. By setting $R_2 = R_1$, $Rth = R_{ref} + dR_{th}$ and $dR_{th} << R_{ref}$, Eq.3.2 can be simplified to

$$V_{diff} \cong -\frac{V_{ref}}{2}\left[\frac{dR_{th}}{R_{th}}\right] \tag{3.3}$$

where dR_{th} is the changing portion of thermistor resistance. Since the thermistor has a negative temperature coefficient of approximately 3%/C^{o} at 25 C^{o} and the reference voltage used is 1.25V, the voltage difference is -18.75 mV/C^{o} at 25 C^{o}. This voltage difference V_{diff} is amplified by a differential amplifier with a gain of 10 and a current limited[1] transconductance amplifier with a conductance of 3.03 A/V to generate drive current for the thermo-electric cooler. This cooler pumps the heat from the laser mounting bracket to the front panel which serves as a heat sink. The efficiency of the cooler is proportional to its drive current. By coupling the temperature dependence of the thermistor with the cooler current, the temperature of the laser diode is indirectly regulated. As the temperature deviates from its set value, the resistance of the thermistor also drifts from its value. This resistance drift will cause a change in the cooler current to compensate the temperature drift.

The open loop gain of the system is calculated to be 0.56 A/C° based on the temperature coefficient and the amplifier gains. The reference resistance is set to 12 kΩ which roughly corresponds to a temperature of 20 C° and the steady state cooler current is recorded at 0.45 A. The steady state temperature error is less than 1 C° around 25 C° according to the loop gain, and the steady state current and the threshold current remains constant within 0.3 mA according to the manufacturer's data[2] [45].

Figure 3.7.a shows the laser temperature with respect to time during power-up with a large initial temperature difference. The laser package was heated to a temperature of approximately 90 C° prior to power up. Figure 3.7.b shows the thermal regulation loop recovering from a thermal disturbance after the laser temperature reaches a steady state temperature.

---

[1] The current limit is used to restrict the cooler current to be within the positive cooling coefficient region. Beyond this region, the heat generated in the cooler will be greater than the heat sinking capacity of the cooler. This current limit is set to be 1 A which is well within the device limit of 2.5 A at 25 C°.

[2] The change in threshold current at 20 C° is extrapolated from the manufacturer's data at 30 - 50 C°.

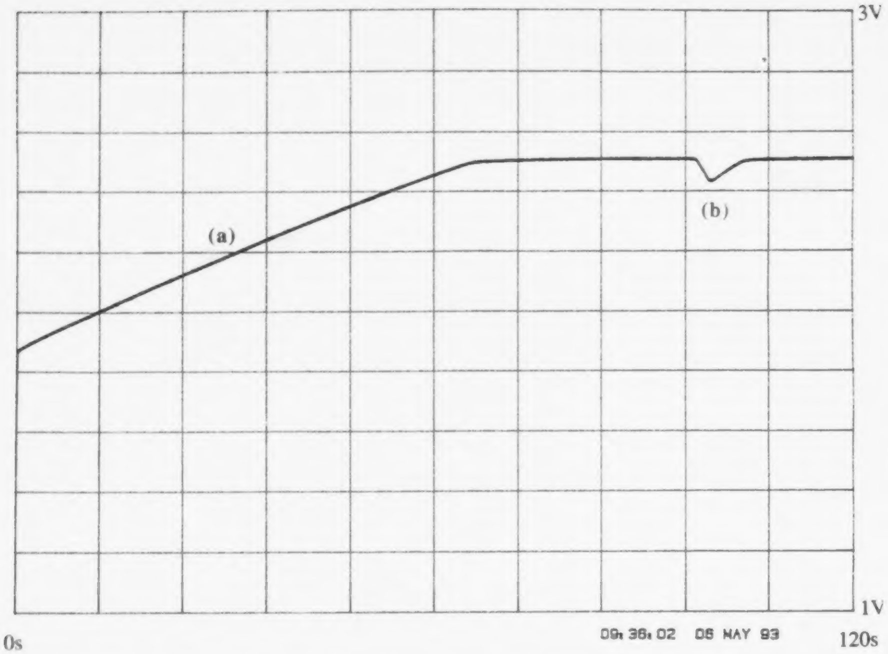


Figure 3.7 The behavior of the laser temperature control loop. (a) The laser diode starts with a 90 C° diode temperature. (b) The laser diode recovers from a temperature disturbance after the diode temperature is already reached a steady state.

3.1.1.3 RF/Bias Insertion Circuit

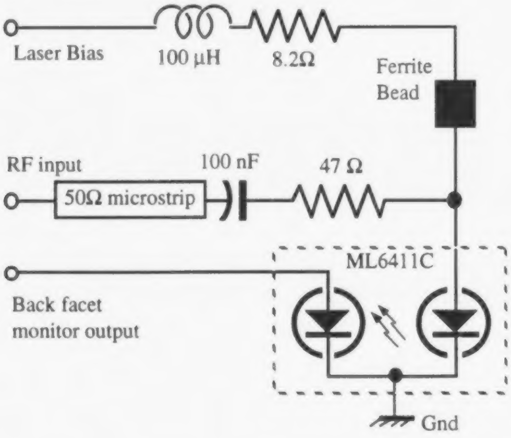

Laser Bias
100 µH
8.2Ω
Ferrite Bead
RF input
100 nF
47 Ω
50Ω microstrip
ML6411C
Back facet monitor output
Gnd

Figure 3.8 Schematic of the bias insertion unit

The purpose of the transmitter is to convert an external RF signal into an optical signal. To achieve this goal, the laser is directly modulated by adding a RF signal current to the DC bias current. An important consideration for the biasing circuit is the fact that the laser diode has a low dynamic resistance under a forward bias: 3 ohm for the

ML6411C. A matching impedance is required when the diode is driven by a 50 ohm external source. Figure 3.8 shows the circuit diagram and the layout of the RF insertion circuit. The circuit is in a biasing tee configuration which provides a high reactance DC path in parallel with a 50 ohm AC path. The high reactance DC path consists of a 100 µH inductor, a ferrite bead and an 8.2 ohm resistor in series. These components serve as low frequency blocking, high frequency blocking, and broadband blocking mechanisms, respectively. The AC path consists of a 50 ohm microstrip with a 100 nF capacitor in series with a 47 ohm resistor. The capacitor isolates the AC path from the DC path; the 47 ohm resistor acts as a broadband matching network to match the low impedance laser diode with the 50 ohm modulation source. Figure 3.9 shows the a measured and the calculated input characteristic of the RF matching network.

The frequency responses of ten laser diodes with the insertion circuit were measured with an Ortel model PD050-OM AlGaAs/GaAs PIN photodiode. The details of the measurement setup and results reported in Appendix E. The 3 dB bandwidth of the laser diodes range from 1.1 to 1.6 GHz; Figure 3.10 shows the frequency response of one of the transmitters. A simulation based on an equivalent circuit consisting of a 3 ohm resistor in series with a 3 nH inductor was conducted and the result is similar in shape to the experimental results[3] but with a higher corner frequency. This lower measured frequency suggests that the lead inductance value was higher than the manufacturer's specification. Further simulation indicates that a higher lead inductance of 6 nH can account for the observed frequency. The additional inductance might be due to the fact that the grounding is via a ground lead instead of via the outer casing which is a common practice in RF circuit applications.

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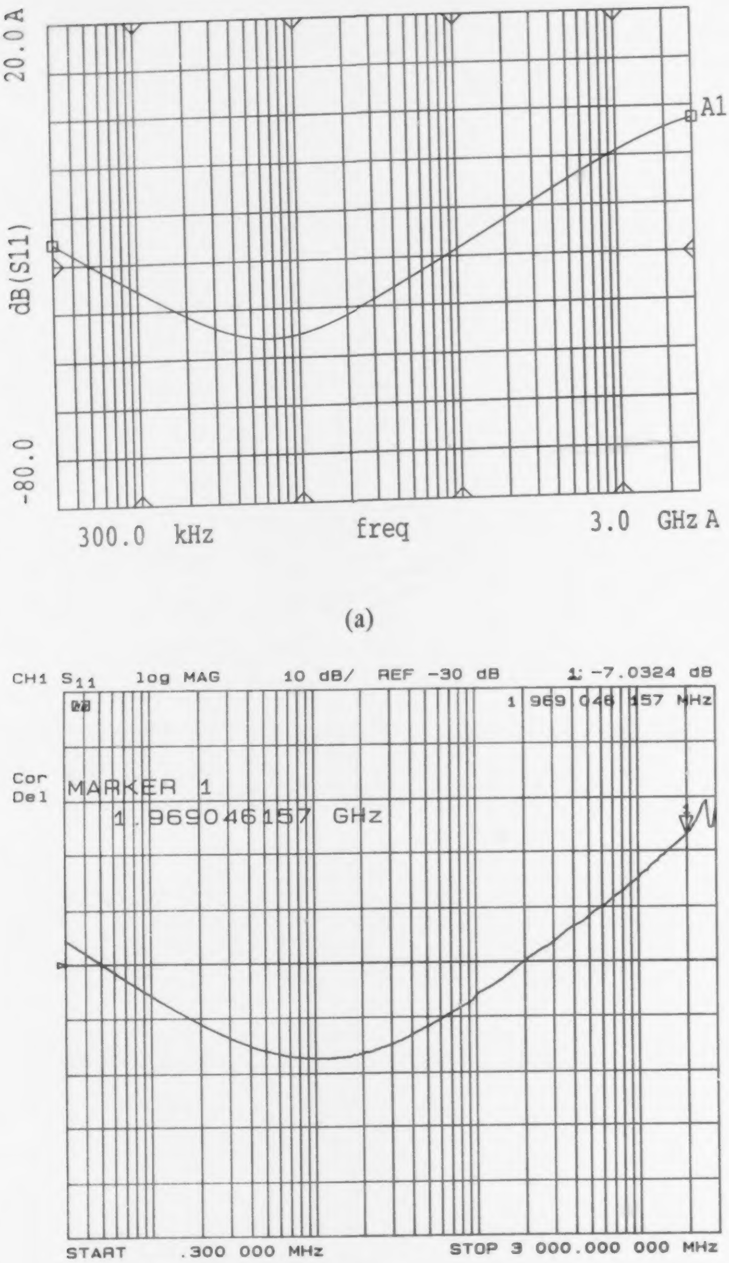
[3] The comparison is done on the transfer functions of the measured signal and the laser current of the simulated circuit.



(a)

(b)

Figure 3.9 The input characteristics of the RF/Bias insertion circuit. (a) simulated result based on a 3 Ω and 6nH laser dynamic model and (b) measured result.

With the same PIN photodiode, the dynamic range of the laser diode was measured to be 131 dB/Hz[4]. This value is slightly higher than the worst case manufacturer specification values of 125 to 128 dB/Hz.

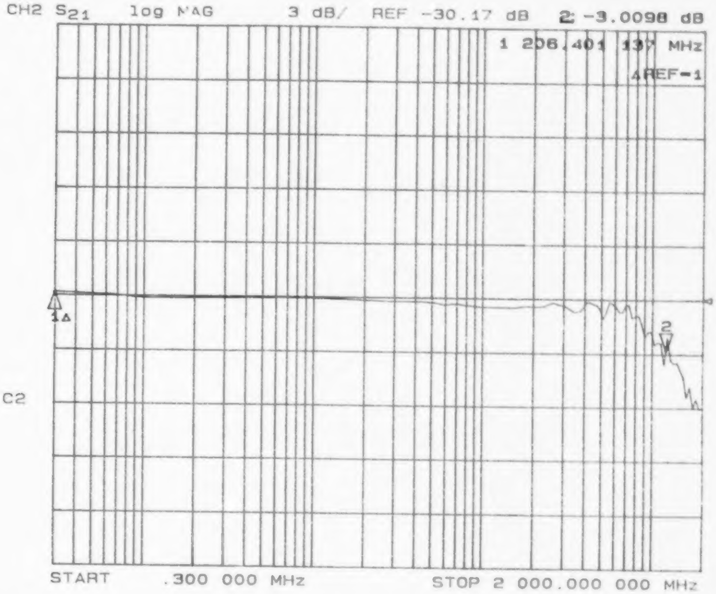


Figure 3.10 The frequency response of Transmitter No.3. The measurement was performed with an Ortel PIN photodiode model PD050-OM with a bias voltage of 25 V and a photocurrent of 0.94 mA.

During the initial testing, a series of noise peaks resembling Fabry-Perot fringes, shown in Figure 3.11, was observed in the noise spectrum of the receiver output. These peaks were removed by injecting index matching oil in the FC connector at the interface of the laser and power splitter. The noise spectrum of a Fabry-Perot laser diode with an external feedback cavity can be affected by optical feedback as low as -30 dB that from an external cavity [44]. The feedback from the FC connector has a maximum end facet reflection of -11 dB with air interfaces, which is sufficient to affect the laser emission spectrum. To avoid the reflection, this connector should be replaced with a lower reflection angled physical contact (APC) connector in the future.

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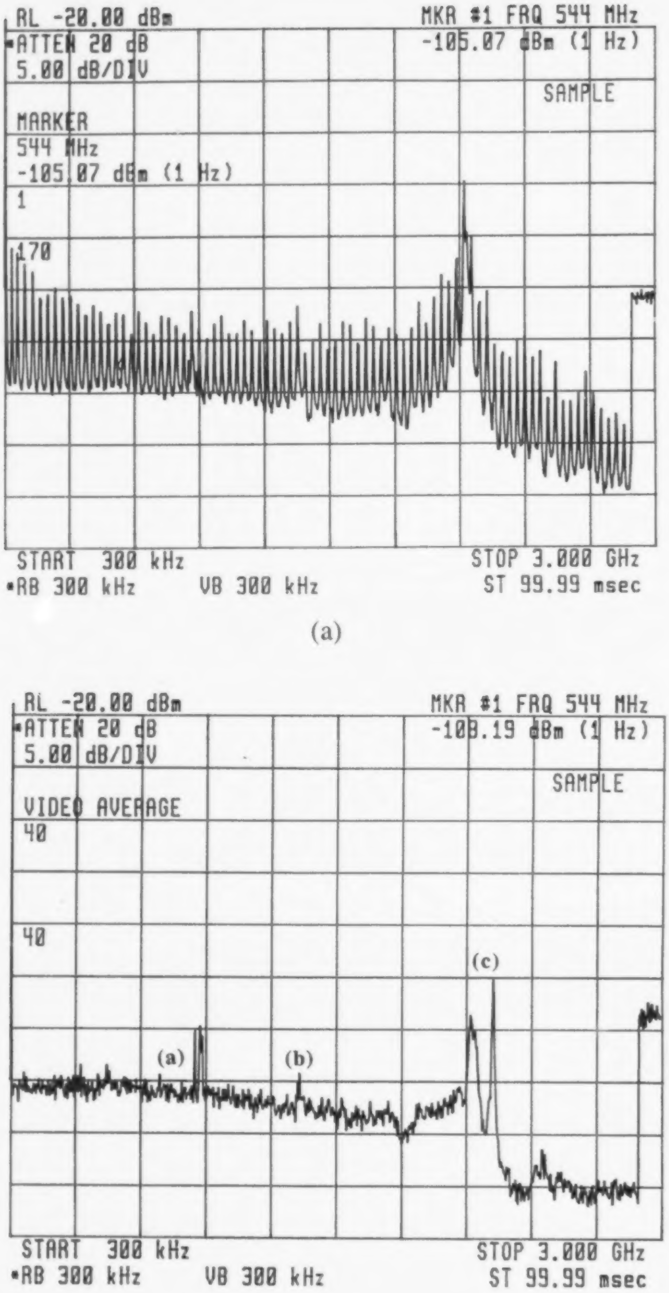
[4] The value is extrapolated from a SNR measurement with a 33% modulation index. The noise floor is not expected to vary with the modulation index.

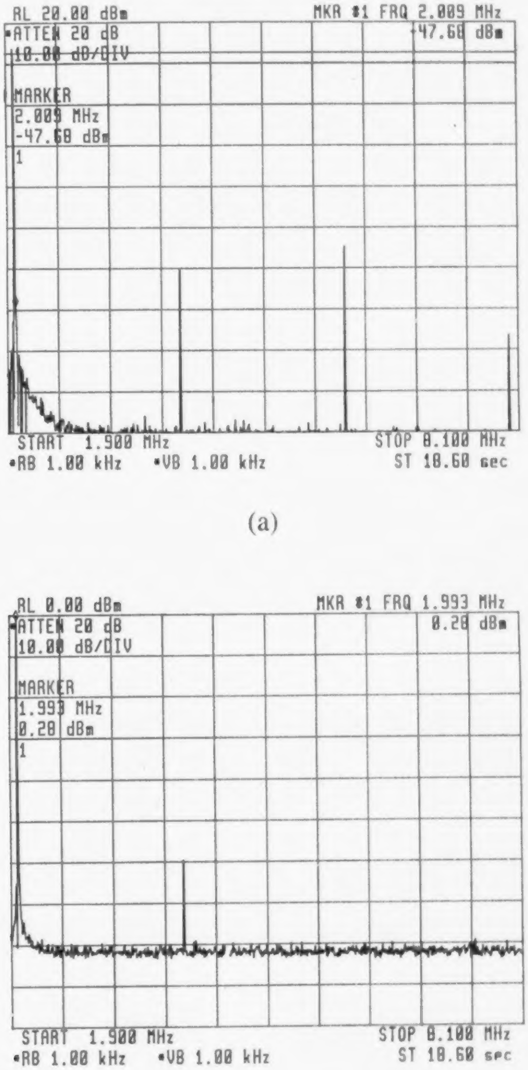


(a)

(b)

Figure 3.11 The effect of the back reflection from a improperly terminated FC connector. a) The noise spectrum with the defective connector. b) The same spectrum after index matching oil is added between the FC connector interface. Note that the large noise peaks near (C) 2.1 Hz are caused by the instability of the receiver amplifier and noise peaks near (A) 0.9 GHz and (B) 1.3 GHz are caused by radio interference from broadcast signals.

The linearity of the transmitter card under different modulation levels is recorded in Figure 3.12[5] . With a 10 dBm (100% modulation index) input, the second harmonic is about 54 dB below the fundamental signal but the third harmonic is only 48 dB below the fundamental signal. With a 0 dBm input, the second harmonic is 59 dB below the fundamental signal with no other observable higher harmonics.



(a)

(b)

Figure 3.12 The linearity measurement of transmitter card No.2 with a 22 dB post-amplifier. a) 14 dBm modulation power. b) 0 dBm modulation power.

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[5] see Appendix E for detailed experimental setup

3.1.2 Laser Housing

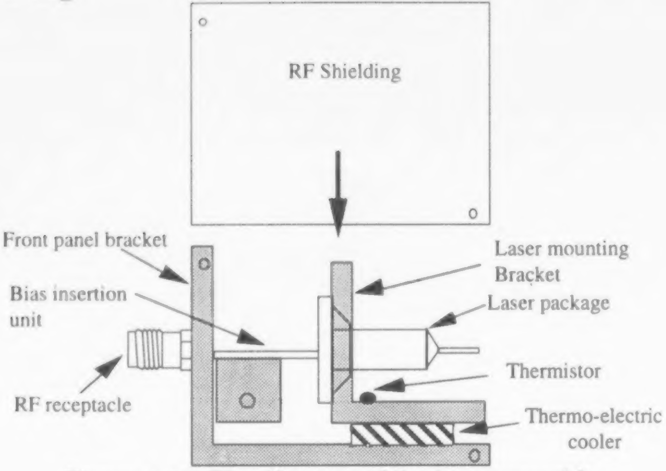

Figure 4.13 The diagram of the laser assembly.

The laser housing is an assembly of mechanical parts to support the laser package and the RF insertion circuit, and to insulate the laser thermally from the rest of the circuit board. The laser housing assembly, shown in Figure 4.13, consists of: the laser mounting bracket, front panel brackets, and sheet metal shielding. The laser is mounted on the smaller laser mounting bracket which then sits on top of a thermo-electric cooler. The RF insertion circuit is situated between the two brackets and connects the RF receptacle from the front panel bracket to the laser package on the laser mounting bracket. To minimize the heat load to the cooler, the laser is thermally isolated from the rest of the assembly and contacts between the laser and the other parts of the assembly are restricted to the insertion circuit and the cooler. Finally, the whole assembly is covered with a sheet metal shield to reduce electromagnetic radiation.

The detailed mechanical drawings and the assembly diagram of the laser housing are listed in Appendix F.

3.1.3 Optical Distribution And Optical Delay

Figure 3.14 illustrates the flow of the optical signal. The optical signal from the laser diode is fed through the reconfigurable delay line and then is coupled into the 1x10 star coupler. The delay line is used to select the relative delays among transmitters. The length of these delay lines depends on the overall system configuration which changes depending on the application. A 1x10 biconical taper fiber coupler splits each optical signal into 10 identical signals. These identical signals are then directed into 10 output optical receivers housed in the receiver module, connecting through the optical backplane.

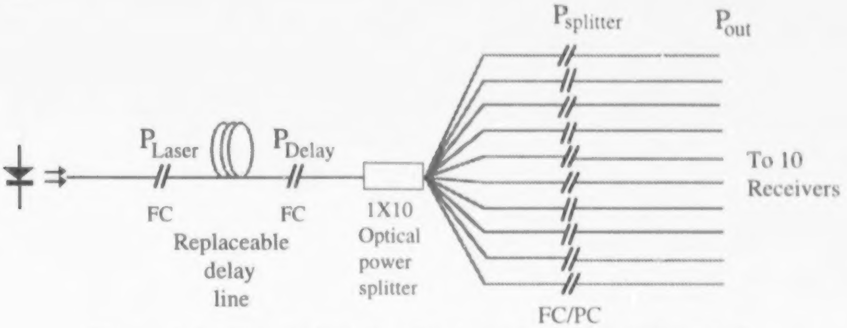

Figure 3.14 The optical distribution of a transmission card.

The optical power levels among the typical optical paths were measured and are listed in Table 3.1. Figure 3.14 shows the positions of the different optical power measurements recorded. The uniformity of the optical outputs is within 1 dB and the splice losses average to -0.2 dB over 11 splices. The insertion loss of the optical splitter is less than the specification by about 1~2 dB. The overall optical system has an average loss less than 12 dB which is less than the expected value of 15 dB. This lower insertion loss may be partly due to the short fiber length, which does not allow the cladding modes to be properly stripped from the fiber.

Table 3.1 Measured optical power levels and losses of a typical transmitter card.

P_{Laser} (mW)	P_{delay} (mW)	Splice loss (dB)	$P_{splitter}$ (mW)	Split loss** (dB)	P_{output} (mW)	Splice loss (dB)	Overall insert-ion loss (dB)
4.97	4.64	0.31	0.36	11.1	0.35	0.12	11.5
			0.37	10.1	0.34	0.36	11.7
			0.40	10.7	0.36	0.40	11.4
			0.41	10.5	0.40	0.10	11.0
			0.40	10.6	0.39	0.10	11.1
			0.42	10.4	0.40	0.20	11.0
			0.41	10.5	0.40	0.10	11.0
			0.37	11.0	0.34	0.37	11.7
			0.38	10.9	0.37	0.10	11.3
			0.45	10.1	0.42	0.30	10.7
**Note: This value includes the insert loss due to the input optical connector.							

An attempt to measure the modal noise contribution of the optics was made using an MSM receiver with a noise figure of 6 dB and a gain of 60 dB. The amplifier noise dominates the noise floor and high frequency modal noise was not observed. To study the modal noise of the optical system, a low noise optical receiver is required to isolate these noise components.

A low frequency mode selective coupling (i.e. low frequency modal noise) was observed to exist over +/- 0.25 dB on a 200 MHz modulation signal over a 60 second period. Figure 3.15 shows a plot of the 200 MHz output over a 60 second period. This effect was suggested to be caused by the mode hoping of the laser coupled with the multimode power splitter [8].

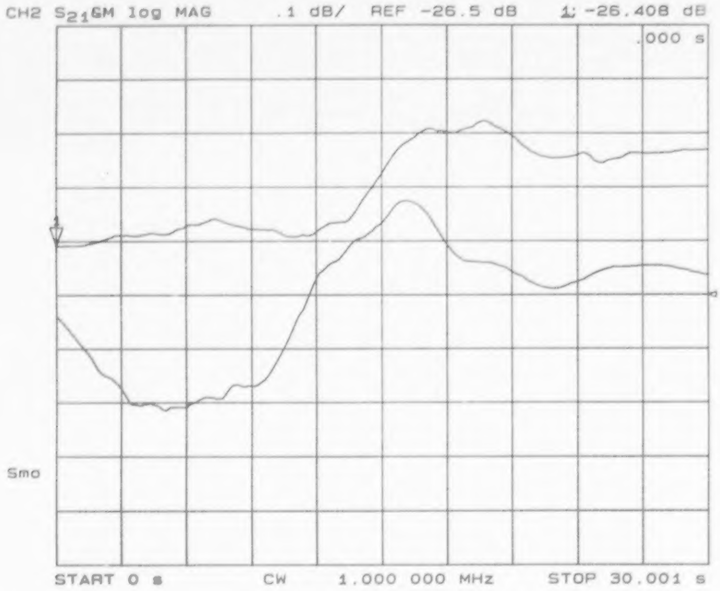

Figure 3.15 The low frequency fluctuation on the optical output of transmitter No.3 (Tx#3).

4.0 RECEIVER MODULE

4.1 Receiver Module Organization

The functions of the receiver module are fourfold: to convert the optical signal back into an electrical form, to perform the optoelectronic weight setting, and to provide access for setting the bias of each crosspoint, and to amplify the detected signal back to the input level. Functionally, this receiver module is divided into two subsystems: the crosspoint bias system and the MSM optical receiver. The crosspoint bias system communicates with the external world via an RS-232 serial bus and generates the bias voltage for each crosspoint according to received commands. The MSM optical receiver system performs the optoelectronic conversion and provides amplification to compensate for the various losses along the optical link.

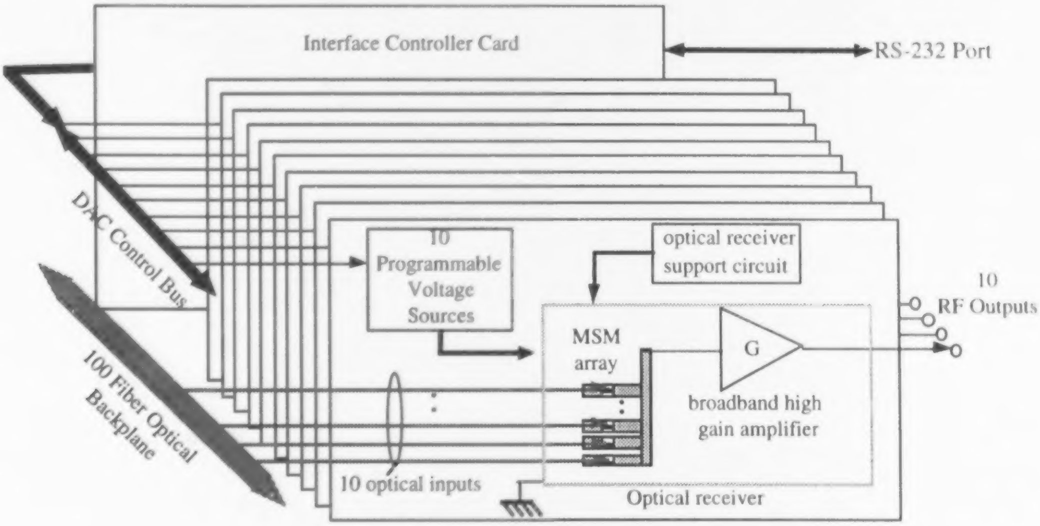
Interface Controller Card
RS-232 Port
DAC Control Bus
100 Fiber Optical Backplane
10 Programmable Voltage Sources
optical receiver support circuit
MSM array
G
broadband high gain amplifier
10 optical inputs
Optical receiver
10 RF Outputs

Figure 4.1 A schematic of the receiver module

Structurally the receiver module, shown in Figure 4.1, is organized into 10 optical receiver cards and one interface controller card. Each optical receiver card supports one MSM detector array which performs the optoelectronic weight setting function and serves as an output column of the matrix. The interface controller card connects to the matrix via a serial port. All these cards are housed in a standard 84 HP 3U Eurocard card cage. Electrically these cards are connected to a 19 bit digital bus and a DC power supply bus; optically each card is connected to the optical backplane of the transmitter module via a bundle of 10 optical fibers.

4.2 Crosspoint Biasing system

The crosspoint biasing system of the receiver module performs two functions. First, it generates 100 independently accessible bipolar voltages for modulating the responsivity of each MSM detector of the 10, 1x10 detector arrays. Second, it provides a simple interface for the external world to set each crosspoint bias.

A simple scheme of microcontroller and programmable voltage sources is used to fulfill these two requirements. A set of 10 programmable voltage sources is located on each receiver card and each source is assigned a unique address which can be accessed independently. These 100 voltage sources are connected to a 19 bit digital bus which is driven by the interface card. Inside the interface card, a microcontroller is programmed to accept commands from an external source via an RS-232 serial bus and then translates these external commands into appropriate digital signal sequences to set the voltage sources accordingly.

4.2.1 Requirements For The Programmable Voltage Sources

From the preliminary measurements described in Chapter 2, a residual bias of 10's of millivolts can degrade the isolation of the crosspoint by several dBs. The resolution of the voltage sources must therefore be less than 10 mV to provide sufficient control to extinguish the crosspoint completely. From the measurements in Chapter 2, the DC responsivity of a MSM photodiode saturates at a bias about 2 V and the output voltage must be equal to or greater than 2 V to utilize the full responsivity and bandwidth. The output voltage ranges of the programmable voltage sources are chosen to be +/-5V which are adequate to saturate detector response.

4.2.2 Programmable Voltage Sources

A set of digital-analog converters (DAC) with an internal data latch is chosen for the programmable voltage sources. The internal data latch serves as a memory to hold the input data until the output requires to be modified. This method eliminates the need for periodic updating in a sample-and-hold scheme used in a previous implementation of a transversal filter [8] and thus decreases the possibility of switching transients leaking into the output voltages. A 12 bit resolution at +/-5V is selected to provide an incremental resolution of 2.4 mV which provides adequate bias resolution to turn off the detectors.

The DAC chosen for this application must satisfy three requirements. First, it must be compact in size into to fit into the limited space on each card. Second, it requires a minimum number of control signals to simplify the control bus requirement. Third, it must match the requirements for the operation of the MSM array which are a resolution less than 10 millivolts and an output range of +/-5V.

The DAC selected for this project is Analog Device 7237 dual 12-bit DAC with a microprocessor compatible interface[1]. This device contains two 12 bit DACs with a shared 8 bit multiplexing data bus which reduces the number of required control signals of the DACs to 11 bits. Its double buffered output allows the internal data to be modified without affecting the current output and enables the synchronized updating for all the crosspoints. This synchronized updating minimizes the ambiguity states during the switching transition. Beside the multiplexing bus and double-buffered output, AD7237 has additional analog features, such as an output current-to-voltage converter, a built-in offset resistor network, and a buffered reference voltage source, that enable the device to function without any additional support circuit. However, under this stand-alone mode, the output voltage of the DAC is not adjustable and is subject to the fluctuation of the internal reference as ambient temperature changes. This fluctuation can lead to 5 LSB bits drift on a full scale output over the operation temperature range (50C° - 0C°) [53]. This drift can be corrected by applying a software offset on the digital input value. This device operating under the stand-alone mode, shown in Figure 4.2, can generate two 12-bit resolution +/-5V output voltages without any additional support circuit.

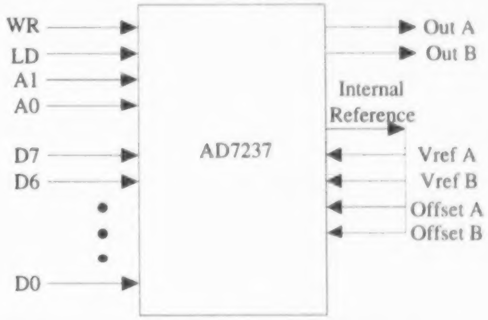

Figure 4.2 A schematic diagram of AD7237 DAC configured in the stand-alone mode

4.2.3 Address Decoder Circuit

A requirement for the bias system is to provide individual access to each crosspoint. This individual access is achieved by assigning an unique address to each DAC. The address selected for this scheme is 9-bit BCD code address. The top four address bits define the position of a receiver card; the next four address bits define the position of DAC within a given receiver card. The last bit indicates the upper byte or the lower byte of the 12 bit data word. A write bit (WR) used to validate the data on the data lines.

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[1] See Ref[54] for detail discription.

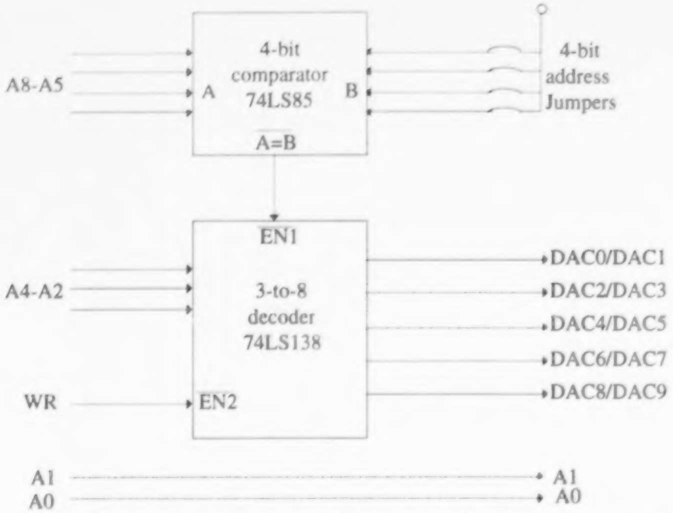

Figure 4.3 A schematic diagram of the address decoder of a receiver card

Figure 4.3 is a schematic diagram of the address decoder section on the receiver card. A 4 bit digital comparator, 74LS85, is used to compare the top four bits (A8-A5) of the address bus against a 4-bit jumper setting. These jumpers are used to program the address of a receiver card and thus allow the receiver cards to be interchangeable. When the upper address is matched the jumper setting, a 3-to-8 decoder 74LS138 is enabled to decode the lower 4 bits (A4-A1) of the address bus. 74LS138 sends an enable signal to the appropriate dual DAC according to the lower 4 bit address code, once the write enable bit (WR) has validated the content of the data bus.

Figure 4.4 is a timing diagram of an operation cycle of the control bus. First, a lower 8 bit data segment and the 9 bit address code with the LSB, A_0, set to low appear on the control bus. Once the data and address bits have settled, the write control line (WR) is asserted low for a minimum period of 150 ns and the data is latched into the input buffer of the DAC. Next, the upper 4 bit data segment is loaded into the data lines and the A_0 is changed to high. Then WR is asserted low once again. This cycle is repeated on each of the DACs requiring updating. Once all the DACs are updated, the new 12-bit data words can be transferred from the input buffers into the output buffers by asserting the load control line (LD) low and the analog outputs of the DACs are updated simultaneously.

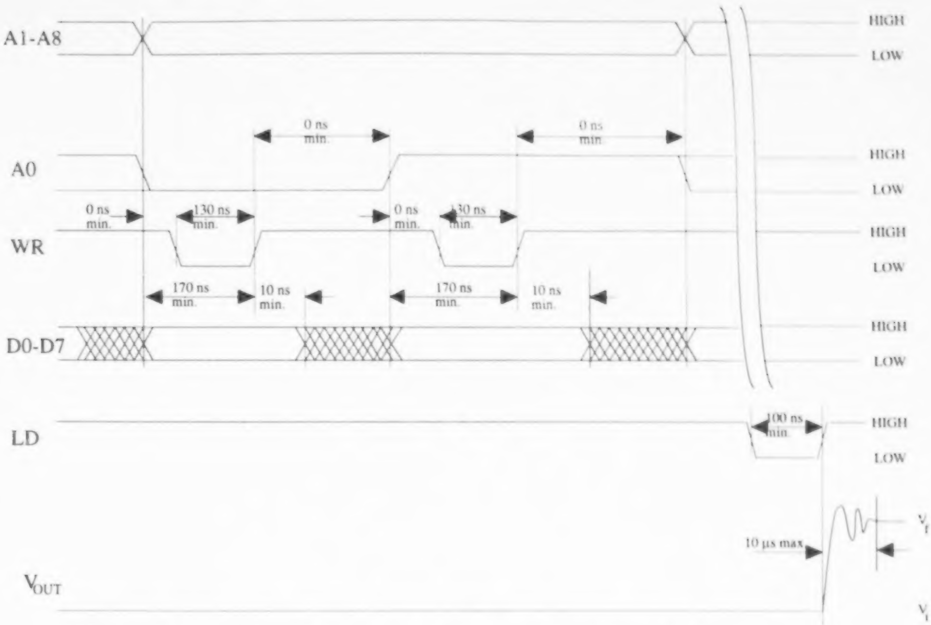
A1-A8
A0
WR
D0-D7
LD
V_{OUT}
HIGH
LOW
0 ns min.
130 ns min.
170 ns min.
10 ns min.
100 ns min.
10 µs max
V_f
V_i

Figure 4.4 a timing diagram of the control bus for the biasing system.

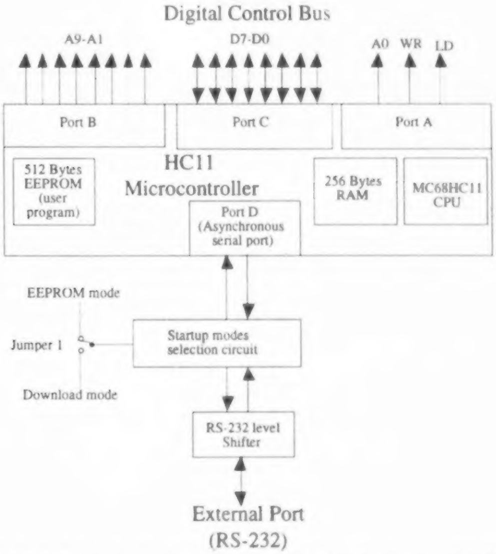
Digital Control Bus
A9-A1
D7-D0
A0
WR
LD
Port B
Port C
Port A
512 Bytes EEPROM (user program)
HC11 Microcontroller
256 Bytes RAM
MC68HC11 CPU
Port D (Asynchronous serial port)
EEPROM mode
Jumper 1
Download mode
Startup modes selection circuit
RS-232 level Shifter
External Port (RS-232)

Figure 4.5 A block diagram of the interface controller card.

4.2.4 Interface Controller Card

An interface card is used to connect the bias system with the external world. The function of the interface card is to translate the external commands into the appropriate digital signals required by the control bus. The interface format between the external source and the matrix is an RS-232 serial format which is compatible with most computing equipment; however, the serial format is intrinsically slower than parallel communication formats.

The block diagram in Figure 4.5 shows the interconnections of the interface controller card. The interface card is based on a Motorola HC11 microcontroller with 625 bytes electrically erasable read-only-memory (EEPROM), 24 programmable I/O lines (port A-C), a synchronous/asynchronous serial port and a programmable baud rate generator [2]. The I/O lines are programmed to drive the digital control bus; the serial port used to handle RS-232 serial interface. The EEPROM of HC11 can be programmed with a single 5V power supply which enables the controller to be programmed in circuit through a RS-232 port[3]. The detailed circuit of the controller card and the pin assignments of the controller are listed in Appendix G.

4.2.5 Control software

Figure 4.6 shows a flow diagram of the software used to control the interface card. This program is listed in Appendix H under the file name of CNTL.ASM. After the power up, the internal program embedded in the controller checks the mode selection bit setting and execute one of the two possible modes: EEPROM mode or download mode[3] . Under the normal operation of the controller, the EEPROM mode is selected and the program starts by initializing all ports appropriately. Next, the program resets every DAC to 0 volts which corresponds to a hexadecimal value of $7FF. Then the program jumps into an infinite loop to wait for a command from the serial port and to execute the command accordingly. In the current version of the program, only two valid commands are used to control the switch: SET and RESET-ALL. The formats of the two commands are listed in Figure 4.7. The SET command reads a valid DAC address and a 12 bit hexadecimal voltage value and sets the specified DAC with the given voltage value. The RESET-ALL command sets all 100 DAC outputs to 0 volt.

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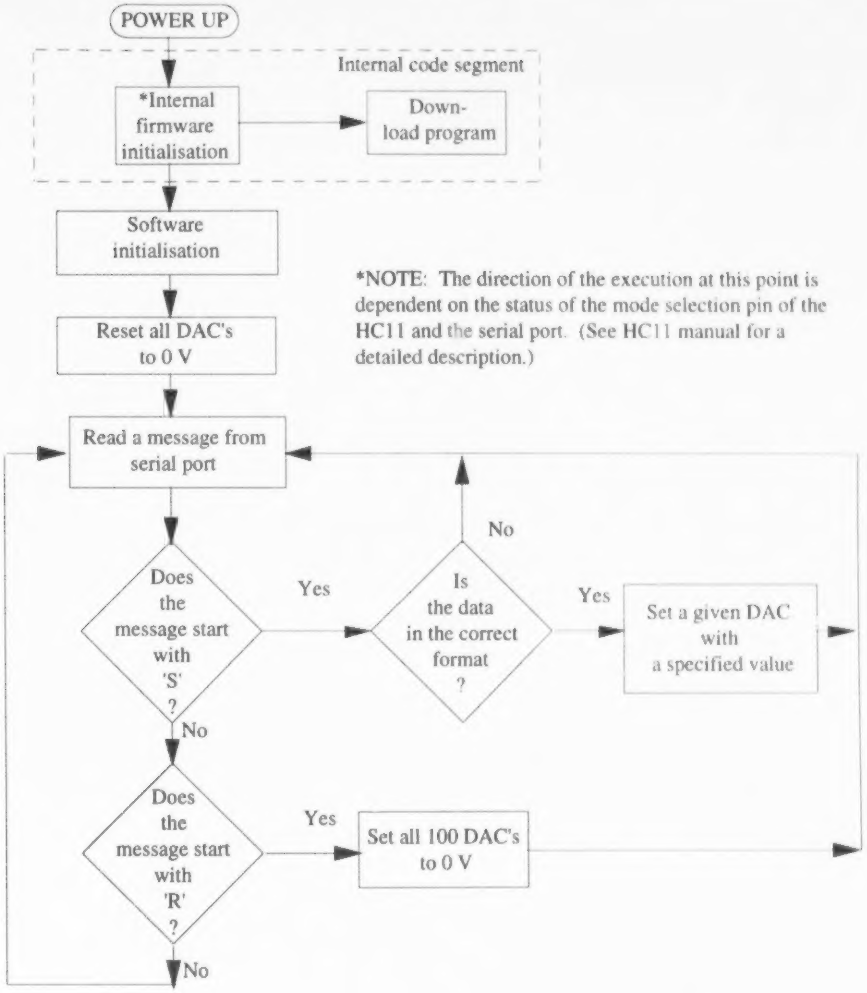
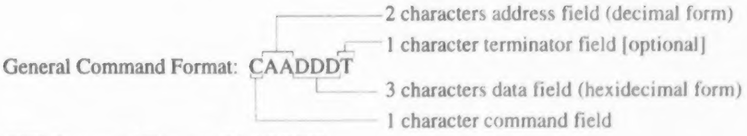
[2] See Ref[55] for the detail description .

[3] See Appendix H for the details on the in-circuit programming procedures.


POWER UP
Internal code segment
*Internal firmware initialisation
Down-load program
Software initialisation
Reset all DAC's to 0 V
Read a message from serial port
Does the message start with 'S' ?
Yes
No
Is the data in the correct format ?
Yes
No
Set a given DAC with a specified value
Does the message start with 'R' ?
Yes
No
Set all 100 DAC's to 0 V

*NOTE: The direction of the execution at this point is dependent on the status of the mode selection pin of the HC11 and the serial port. (See HC11 manual for a detailed description.)

Figure 4.6 An execution flow diagram of the HC11 control program for the biasing system


2 characters address field (decimal form)
1 character terminator field [optional]
General Command Format: CAADDDT
3 characters data field (hexidecimal form)
1 character command field

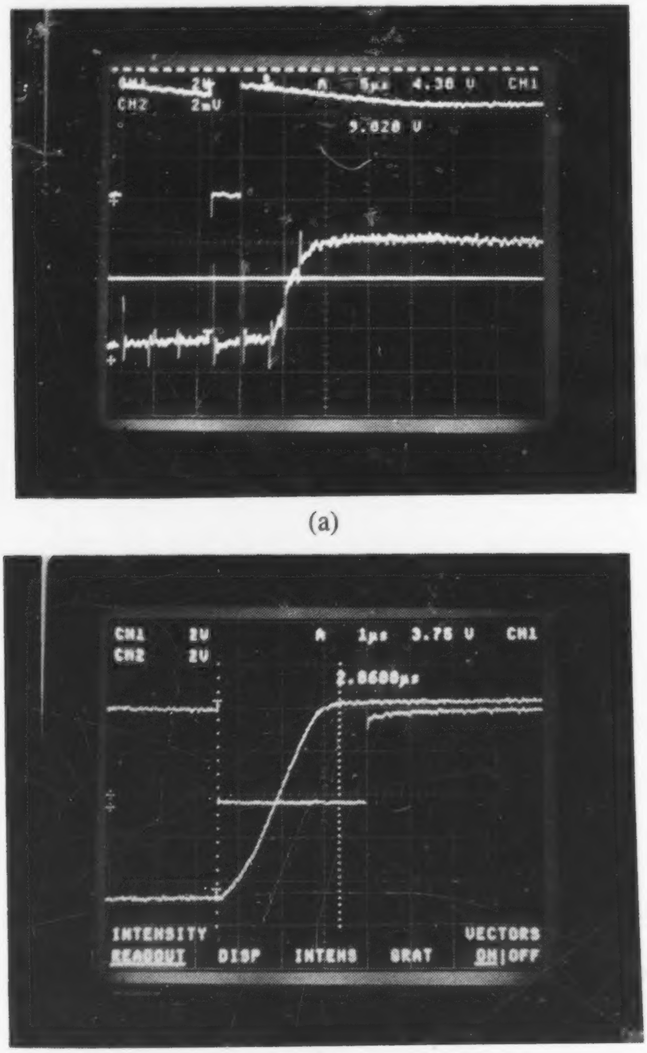
SET Command Format: SAADDDT

RESET-ALL Command Format: RT

Figure 4.7 The command format of the interface controller card

4.2.6 DAC bias system performance

Figure 4.8 shows the switching transient of an AD7237 output and the LD pulse measured with Tektronix 2430 digital oscilloscope. Note that a 6 mV noise voltage spike from the digital circuit is superimposed on the output voltage during the transition of LD pulse. This spike is of the same order as the voltage resolution of the DAC. The rise time for a full 10 voltage output swing from -5 to 5 V was measured to be 2.8 µs which is well within the 10 µs specified.



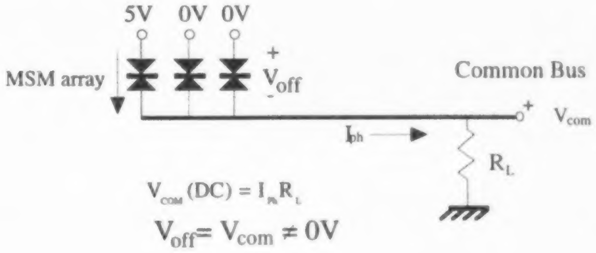
(b)

Figure 4.8 The switching transient measurements of the biasing circuit. a) The switching transient of a 2 LSB output Voltage and the WR pulse. b) The switching transient from -5 to 5 V output swing and the LD pulse.

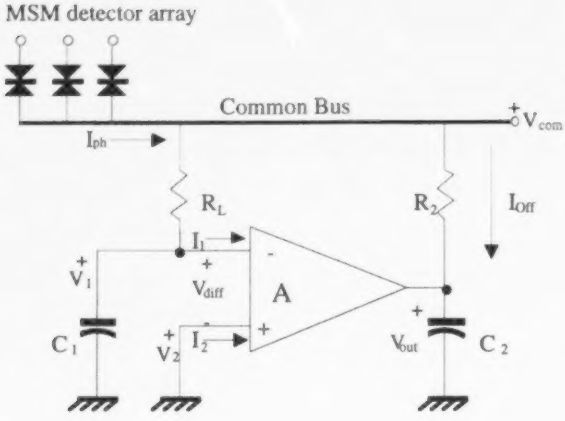
4.3 Miscellaneous Optical Receiver Support Circuits

Another function for the bias card is analog support: the receiver power supply and virtual ground locking circuit. To increase the immunity to digital switch noise from the digital circuits, the optical receiver is supplied by a set of voltage regulator circuits which are separated from the digital power supply. This voltage regulator removes any voltage parasitic transient generated by the digital circuit from the power supply of each optical receiver.

One consideration during the optical receiver design is that the photocurrent from individual MSM photodiode passing through the common load resistance can induce an offset voltage on the common bus of the detector array. Figure 4.9.a depicts this problem. The offset voltage forms a small bias across the normally unbiased detectors and thus renders them partially sensitive. To overcome this problem, a virtual ground circuit is added to regulate the DC component of the common bus to remain near 0 V [36]. Figure 4.9.b illustrates the schematic of the virtual ground circuit, which consists of one operational amplifier (OP-AMP) and two resistors, and its principle of operation. The common bus of photodetector array is connected to the two resistors of a negative feedback loop. The feedback action of the operational amplifier transforms the common bus into a virtual ground. This feedback action is limited to low frequency by introducing two capacitors to decouple the feedback loop and a compensation network to reduce the bandwidth of the operational amplifier to avoid oscillation.



(a)



Assumptions: $I_1 = I_2 \approx 0$

$A \rightarrow \infty$

For $A \rightarrow \infty$,

$$V_{out}(DC) \rightarrow (V_2 - V_1) \approx 0$$

$$\therefore V_2 \approx V_1$$

$$\therefore V_{com} = V_1 + I_1 * R_L$$

$$I_1 \approx 0 \quad \text{and} \quad V_1 \approx V_2 = 0$$

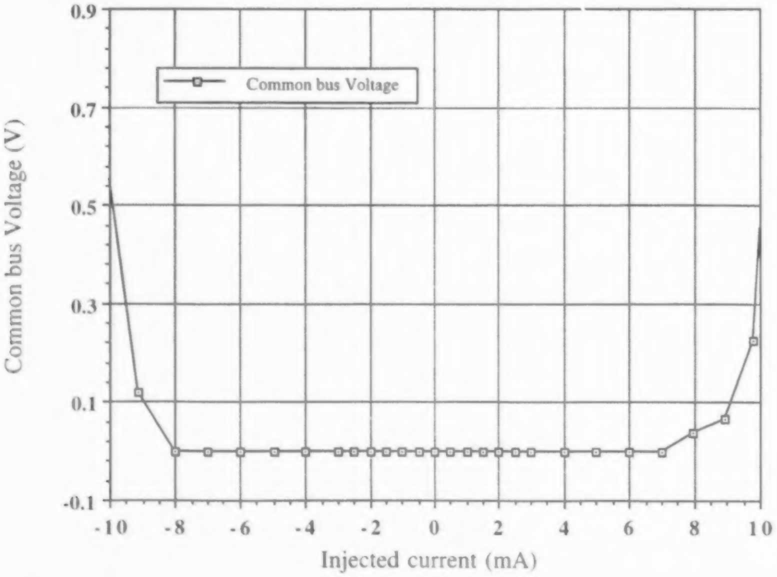
$$\therefore V_{com} = 0 \ ; A \rightarrow \infty$$

$$; I_1 = I_2 = 0$$

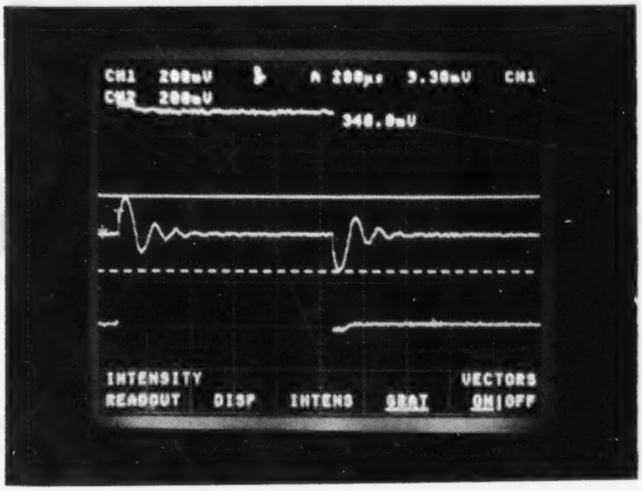
(b)

Figure 4.9 The DC photocurrent interference on a MSM photodiode array. (a) The effect of the DC photocurrent on the unbiased detector. (b) The virtual ground circuit and its operation principle.

Figure 4.10.a shows the relationship between the current injected and the bus voltage. The virtual ground is maintained for DC injection current between 9 mA and -8 mA. Figure 4.10.b shows the virtual ground voltage when a transient current pulse is injected into the loop. The large trace is the 1 $mA_{p\text{-}p}$ current pulse injected into the common bus and the smaller trace is the 0.3 Vp-p transient voltage developed on the bus. The transient oscillation on the bus voltage is caused by the capacitive loading on the output terminal which may be stabilized by adding a series resistance between the output of OP-AMP and the bypassing capacitor or by reducing the bypassing capacitance.



(a)



(b)

Figure 4.10 The behavior of the virtual ground circuit (a) under a DC current injection, (b) under a periodic injection.

4.4 Planned Optical Assembly Procedures

A Silicon V-groove wafer is used to accurately align the optical signals from ten fibers onto the MSM detector array. This V-groove wafer, manufactured using an Ethylenediamine-Deionized water-Pyrocatecol (EDP) or Ethylenediamine-Pyrocathecol-Water (EPW) anisotropic etching process developed in the Alberta Microelectronic Centre, consists of a set of 10 v-grooves 275 µm in depth. The design of the alignment wafer was modified from an optical fiber ribbon connector designed by Sentil Kumar at TRLabs [55]. Figure 4.11 and 4.12 shows the mask for the wafer with the modifications and a cross-section view of the groove with fibers. The dimensions of the V-grooves allow an optical fiber to be forced inside the groove with a straight edge applied across the top of the wafer. Once a fiber is positioned inside a groove, the fiber is secured by applying an optical epoxy on top of the fiber. The epoxy used is a Norland NOA-68 ultraviolet (UV) light curable optical epoxy. This optical epoxy is dispensed in a liquid form by a computer controlled liquid dispensing unit developed by Dr. Barrie Keyworth at TRLabs. The unit consists of three computer controlled micropositioners with a resolution of 200 nm per step and an electronically controlled dispensing syringe. By controlling the flow rate of the epoxy, and the position and speed of the syringe, an exact amount of epoxy can be dispensed into a precise location. Once the epoxy is dispensed on a fiber, the epoxy is cured by applying a strong UV light. This dispensing scheme allows the fibers to be aligned individually and precisely within +/- 30 μm. Figure 4.13 shows front view of a finished alignment wafer.

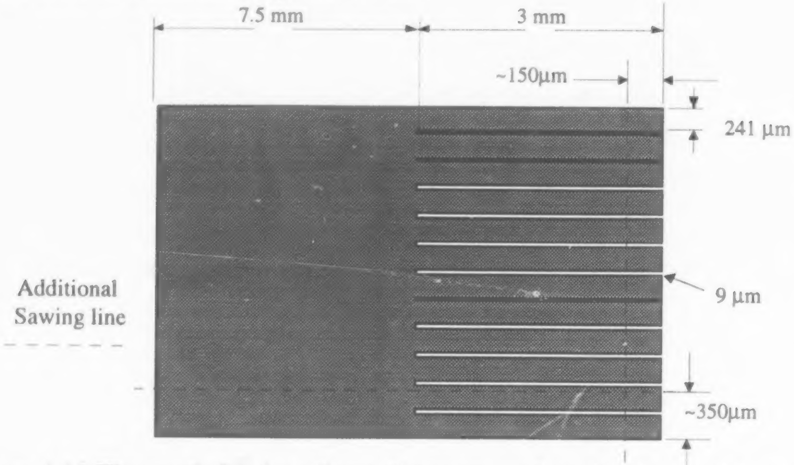

7.5 mm
3 mm
~150μm
241 μm
9 μm
~350μm
Additional Sawing line

Figure 4.11 The mask for the silicon alignment wafer with the modifications

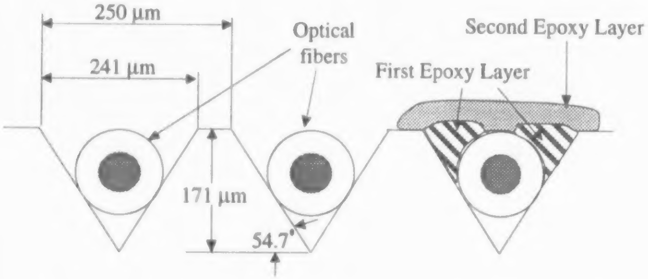

250 μm
241 μm
Optical fibers
Second Epoxy Layer
First Epoxy Layer
171 μm
54.7°

Figure 4.12 The front view of the alignment wafer

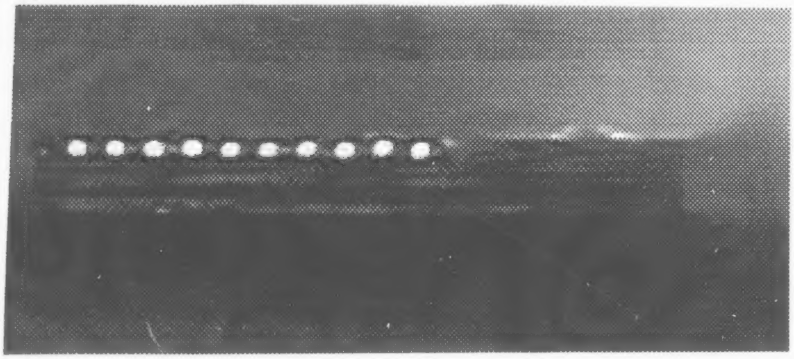


Figure 4.13 A picture of an assembled alignment wafer with optical outputs.

After the fiber bundle with the V-groove wafer is assembled, the assembly is aligned with a vacuum holder setup and micropositioner. An active alignment technique, developed by M. Veilleux in Ref.[30], is used to align the fiber bundle with the detector array. Two optical signals with two different modulation frequencies are launched on the two end fibers of the bundle and the receiver output is monitored with a HP-71000 spectrum analyzer. The alignment is achieved when both signals are maximized and equal.

In this thesis, the emphasis is on testing the performance of the core elements of an optoelectronic processor, and the optical fiber bundle is not fixed to the array with epoxy for these experiments.

In the final assembly, a drop of optical epoxy would be applied to adhere the alignment wafer onto the surface of the detector array once the alignment is achieved. The fiber bundle would be bolted down with two strain release poles and then the vacuum holder would be removed.

4.5 MSM optical Receiver

The optical receiver converts 10 optical signals back into electrical form and amplifies the resulting electrical signal to compensate for the conversion and the optical power split losses and the propagation losses through the system. A MSM photodetector array performs the optoelectronic conversion for the 10 optical signals and a high gain, low noise amplifier is used to compensate the losses. Based on the analysis in Chapter 2, the amplifier requires roughly 60 dB gain to compensate the losses and the minimum bandwidth of 1.2 -1.6 GHz to utilize the full bandwidth of the laser diode.

4.5.1 Original MSM Receiver Design

A 5 stage monolithic microwave integrated circuit (MMIC) amplifier train with two high pass equalization stages was designed to achieve the desired gain and bandwidth. The amplifier consists of two amplifier sections: a 3 stage high gain amplifier and a 2 stage output amplifier. Two simple RC high pass equalization stages were added to compensate any premature roll off of the cascaded amplifier stages. Figure 4.14 shows the complete circuit of the receiver amplifier with the MSM photodiode array.

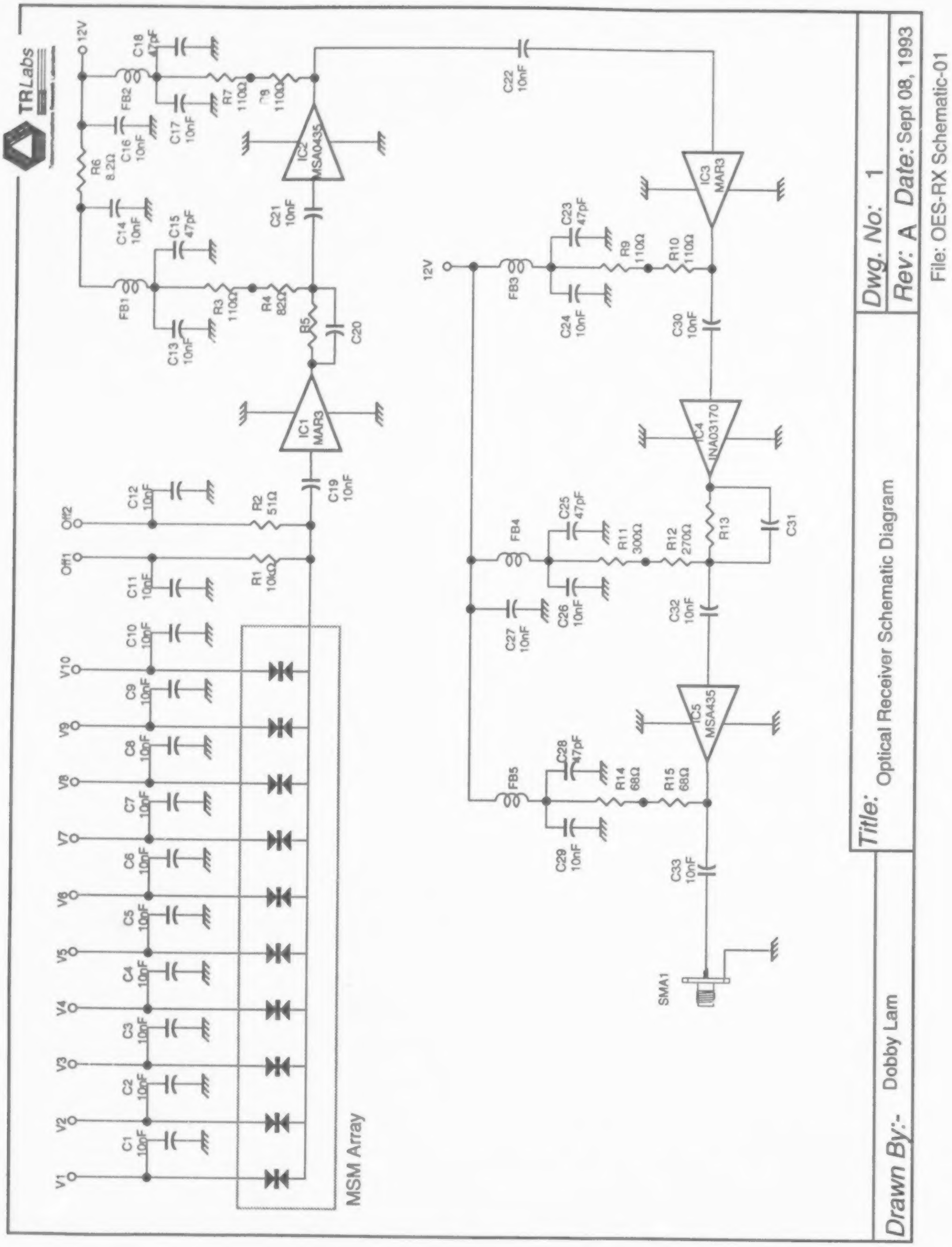

TRLabs
V1
V2
V3
V4
V5
V6
V7
V8
V9
V10
C1 10nF
C2 10nF
C3 10nF
C4 10nF
C5 10nF
C6 10nF
C7 10nF
C8 10nF
C9 10nF
C10 10nF
MSM Array
Off1
Off2
C11 10nF
C12 10nF
R1 10kΩ
R2 51Ω
C19 10nF
IC1 MAR3
R5
C20
R3 110Ω
R4 82Ω
C13 10nF
FB1
C15 47pF
C14 10nF
R6 8.2Ω
C16 10nF
FB2
C18 47pF
12V
C17 10nF
R7 110Ω
R8 110Ω
C21 10nF
IC2 MSA0435
C22 10nF
IC3 MAR3
12V
FB3
C23 47pF
C24 10nF
R9 110Ω
R10 110Ω
C30 10nF
IC4 INA03170
FB4
C25 47pF
C26 10nF
C27 10nF
R11 300Ω
R12 270Ω
R13
C31
C32 10nF
IC5 MSA435
FB5
C28 47pF
C29 10nF
R14 68Ω
R15 68Ω
C33 10nF
SMA1
Title: Optical Receiver Schematic Diagram
Dwg. No: 1
Rev: A
Date: Sept 08, 1993
File: OES-RX Schematic-01
Drawn By:- Dobby Lam

Figure 4.14 A schematic diagram of the original MSM receiver.

After the amplifiers were assembled, a 1x8 1μm MSM photodiode array was mounted and wire-bonded directly onto the receiver circuit card. The completed receiver with the MSM detector array was tested with an optical output from a transmitter card. Several problems were observed during the testing. First, the bandwidth of the receiver was less than the predicted value. Figure 4.15 shows a receiver response which exhibits a low 3 dB corner frequency of 500 MHz. This value is lower than the expected value of 1.2 GHz by a factor of 2. Second, the amplifier exhibits oscillations at both high frequency (1-2 GHz) and low frequency (1MHz). Figure 4.15 illustrates the some of problems of the optical receiver.

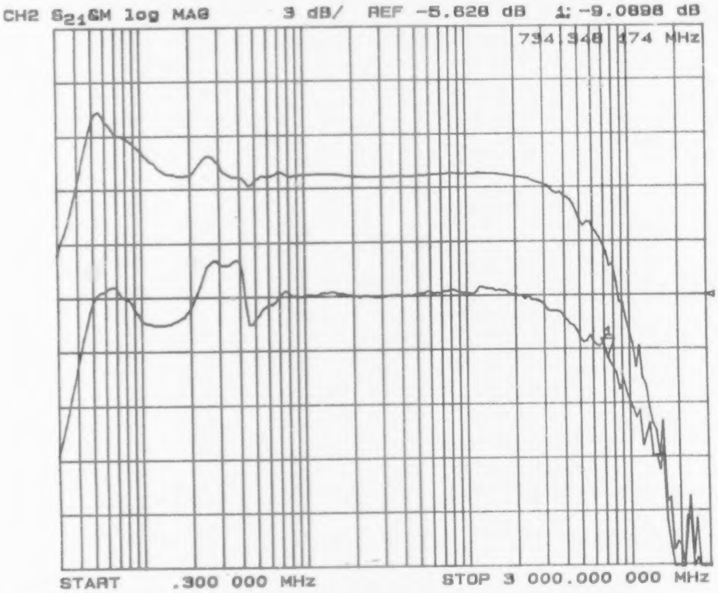
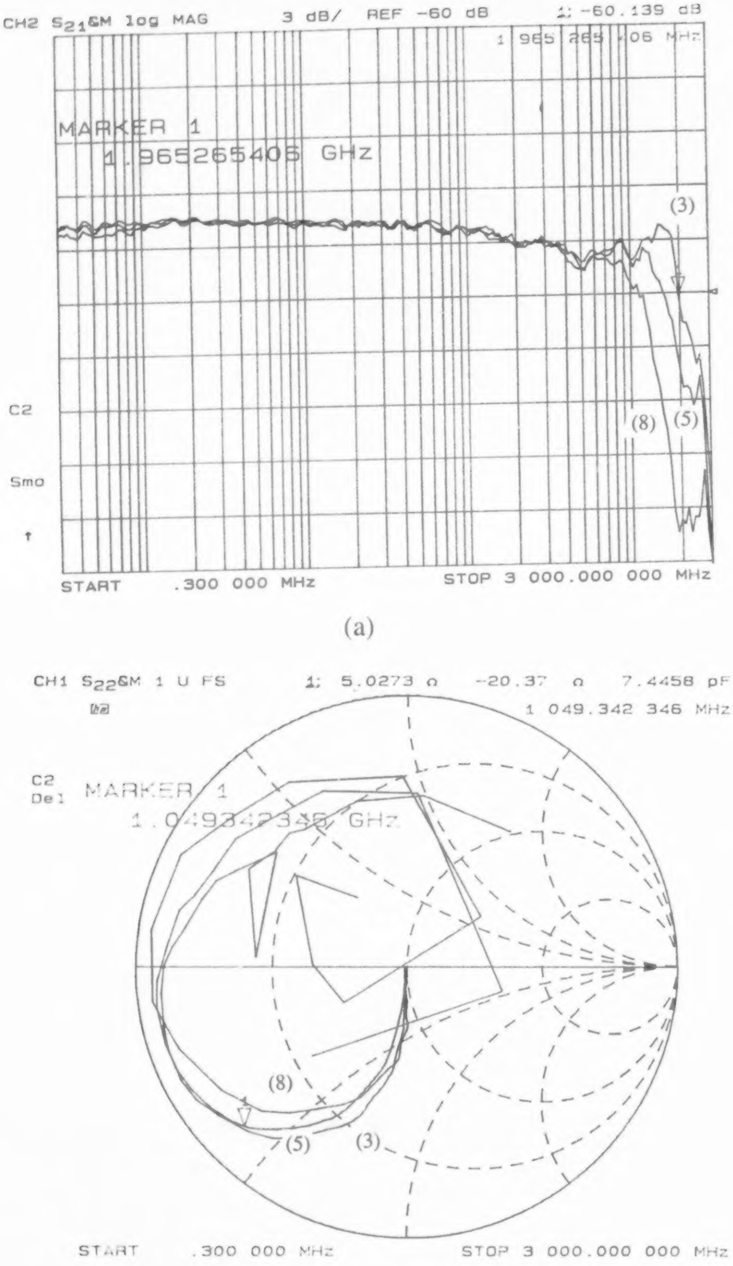


Figure 4.15 Two typical frequency response of the original MSM receiver design with various problems.

After further investigation, the high frequency instability problem of the amplifier was found to originate from poor quality in the printed circuit board, especially on the grounding via. A simulation of the amplifier reveals that the stability of the high gain stage, INA03170, is highly sensitive to the ground inductance which may originate from the poor quality ground via. The low frequency instability was found to be caused by the poor low frequency power supply isolation. The ferrite bead has insufficient impedance to block the lower frequency signal from leaking back into the input signal through power supply line. The problem was remedied by adding a large series inductance (100μH) on the power supply line of each amplifier stage. The low 3-dB frequency response of the overall receiver was found to be caused by the high capacitance of the photodiode array.



(a)

(b)

Figure 4.16 The scatter parameters of the MSM photodiode array with various numbers of photodiodes (3, 5, and 8 detectors per array). (a) S_{21} and (b) S_{22} measurements.

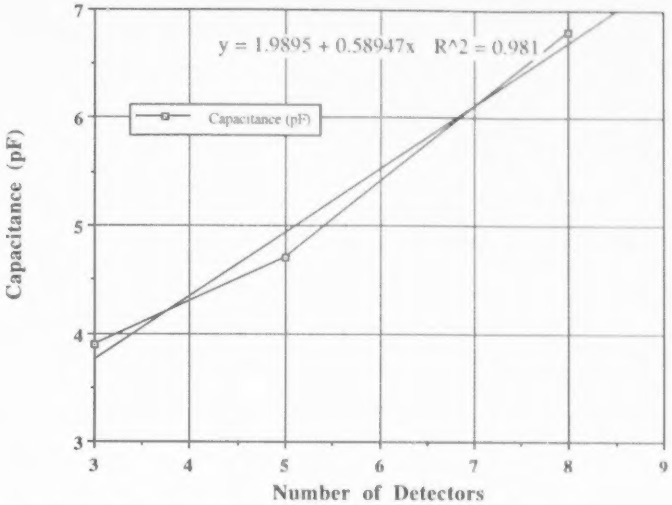


Figure 4.17 The capacitance of 1 μm finger spacing MSM capacitance as a function of the number of photodiodes.

The frequency response and the terminal impedance of a 1μm finger spacing MSM photodiode array with a 51 Ω termination were measured with a HP-8753A network analyzer. Figure 4.16 shows the scatter parameters of the photodiode array with 3, 5, and 8 detectors connected in parallel. Based on the measurements from Figure 4.16.a, the bandwidth of the 10 photodiodes in parallel is expected to be lower than 1 GHz. The lower frequency response is chiefly due to the cumulative capacitance of the photodiode array. The value of the array capacitance was obtained from the S_{11} parameters measurements on Figure 4.16.b. These capacitance values are plotted in Figure 4.17 which shows that the capacitance of the a single 1μm photodiode is about 0.6 pF and the substrate capacitance is about 2 pF. Based on these capacitance values, the capacitance limited bandwidth of a 50 Ω amplifier with a 1x10 array is about 500 MHz. Furthermore, the detector capacitance is expected to increase under illumination because of the photogenerated spatial charge inside the photodiode [56]. A similar 1μm spacing 100μmx100μm MSM photodiode was reported to have a 1.2 pF under a 400 μW illumination [57].

This high photodiode capacitance posts a serious bandwidth limitation for the processor because of the requirements of optoelectronic summing node. Unlike an optoelectronic switch column, an optoelectronic summing node requires multiple photodiodes operating at the same time. Each photodiode represents an input to the summing node. These parallel photodiodes cause a capacitance build up on each node and thus a bandwidth reduction. On the other hand, an optoelectronic switch column requires only one photodiode sensitized at a time. The unused photodiodes can be isolated from the rest of the column by using series switches on the bias lines. Therefore, the capacitance of an optoelectronic switch column is not necessarily proportional to the number of photodiodes in each column. This relationship is advantageous for implementing a large switch matrix.

This capacitance limited bandwidth can be remedied by reducing the photodiode capacitance or lowering receiver input impedance. The capacitance of an interdigitated MSM photodiode is proportional to the area of photodiode and its finger spacing [56]; therefore, the MSM capacitance can be reduced by using a smaller photodiode. A 75 μm x 75μm photodiode, which is large enough to capture most the light from a 50 μm core optical fiber, is expected to have half capacitance of the current 100 μm x 100μm photodiode. Lowering the input impedance of receiver amplifier can also expand the bandwidth of the receiver; however, the low input impedance increases on the thermal noise input and degrades the dynamic range of the system.

4.5.2 Modified Receiver Design

The modified receiver design was intended to overcome the oscillation problem by improving the grounding of the circuit board and by adding the biasing blocking inductance. The amplifier and the MSM photodiode array biasing circuit are mounted on separate circuit board to ensure testability. Also an additional termination resistance was added on the MSM biasing circuit to reduce cable reflection on the connections and the input impedance of the receiver. This termination resistance also decreases the total input impedance from 50 Ω to 25 Ω. This lower input impedance are expected to improve the bandwidth of the receiver and also will increase the thermal noise of the receiver. To compensate for the noise increase, the gain margin of the receiver is reduced and the amplifier gain is set to be about 56 dB which can marginally compensate all the losses.

Two modified receivers shown in Figure 4.18 were built, and their frequency responses and the noise performances were recorded in Figure 4.19. The gains of the two amplifiers are found to be 55 +/-1 dB with a bandwidth of 1.7 GHz and 56 +/1 dB with a bandwidth of 1.6 GHz. The noise floors are roughly -112 dBm/Hz over these bandwidths. These noise floor values are better than the expected value of -107 dBm/Hz which is based on a front end noise figure of 6 dB and a gain of 55 dB. Next, two 1x4 MSM photodiode arrays mounted on rotational stages used to serve as the optical receiver front ends. Two optical fiber bundles and alignment wafers were positioned with two micropositioner to couple the multiple optical signals into the two MSM arrays.

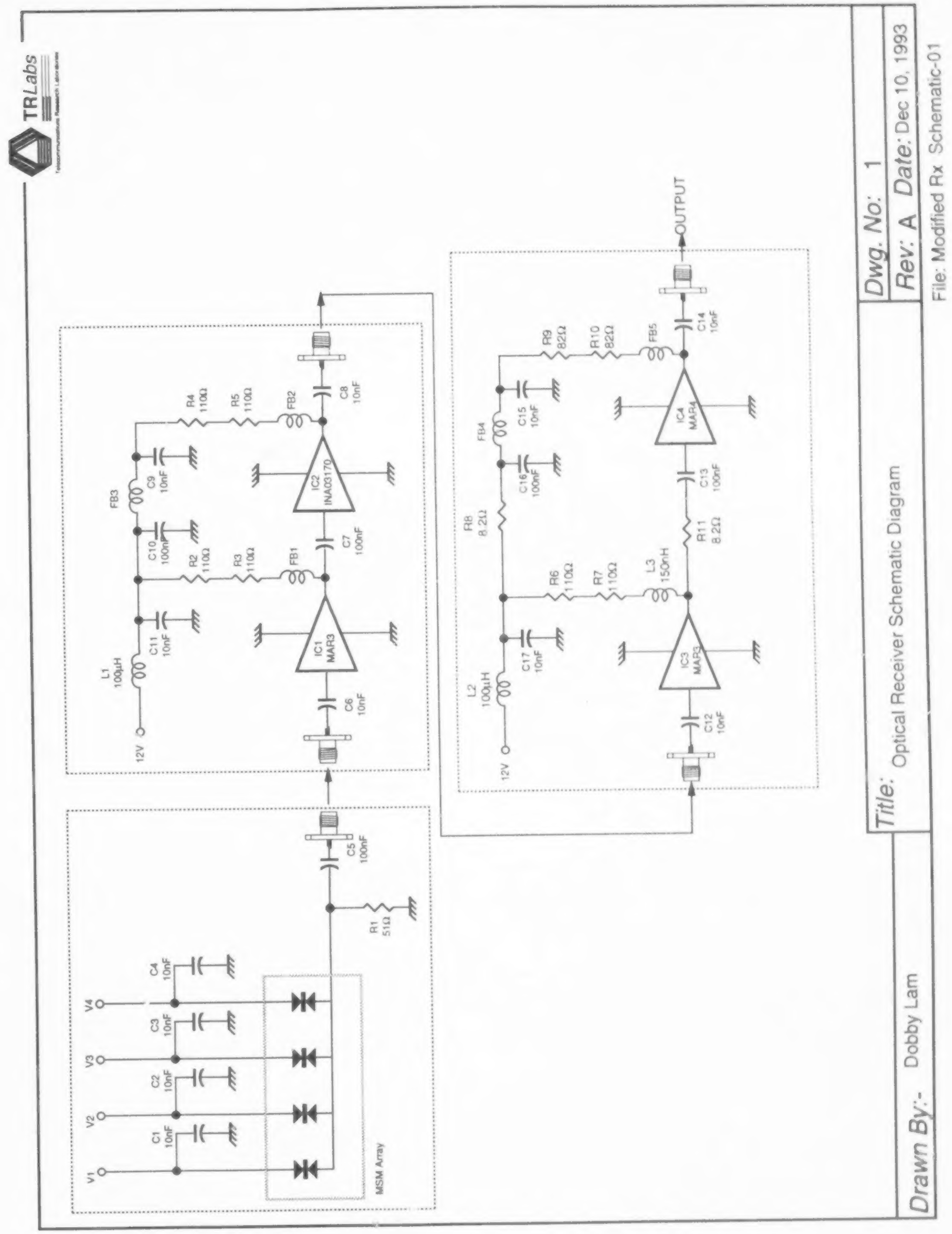
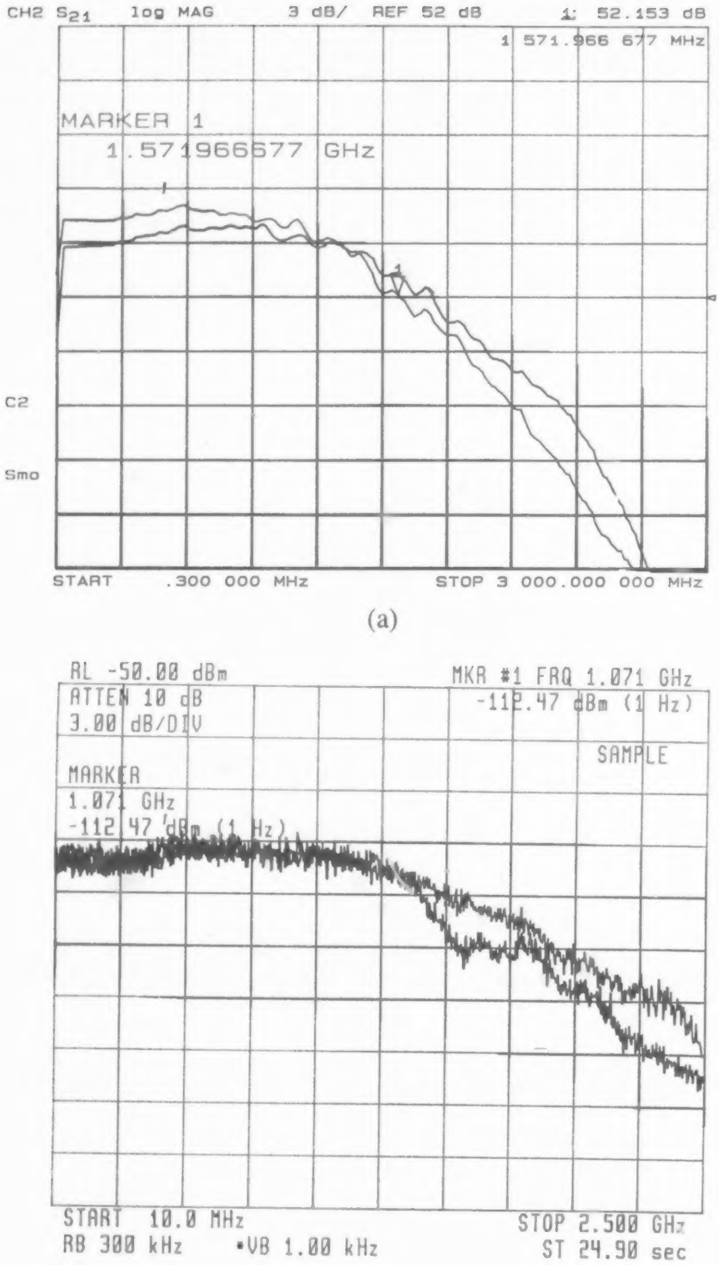

TRLabs
V1
V2
V3
V4
C1 10nF
C2 10nF
C3 10nF
C4 10nF
MSM Array
R1 51Ω
C5 100nF
12V
L1 100µH
C11 10nF
R2 110Ω
R3 110Ω
C10 100nF
FB3
C9 10nF
R4 110Ω
R5 110Ω
FB1
FB2
C6 10nF
IC1 MAR3
C7 100nF
IC2 INA03170
C8 10nF
12V
L2 100µH
C17 10nF
R6 110Ω
R7 110Ω
L3 150nH
R8 8.2Ω
C16 100nF
FB4
C15 10nF
R9 82Ω
R10 82Ω
FB5
C12 10nF
IC3 MAR3
R11 8.2Ω
C13 100nF
IC4 MAR4
C14 10nF
OUTPUT
Dwg. No: 1
Rev: A
Date: Dec 10, 1993
Title: Optical Receiver Schematic Diagram
Drawn By:- Dobby Lam
File: Modified Rx Schematic-01

Figure 4.18 A schematic diagram of the modified amplifier circuit.



(a)

(b)

Figure 4.19 The performances of the two modified amplifiers. (a) the frequency responses and (b) the noise floors.

When the MSM photodiode is under 5 V bias, the two output receivers exhibit bandwidths of 1.2 GHz and 1.5 GHz with +/- 1.5 dB gain ripple. Figure 4.20 shows the frequency responses of the two optical lines (i.e. Tx-Rx pair). The gain ripple is chiefly caused by the two factors: the gain ripples of both MSM and the laser diode responses and the long cable length connecting the components. The long cable in conjunction with the fact that the system is not exactly matched leads to reflections and thus an increase on gain ripple. From Figure 4.16.a, the combined response of a 1x5 MSM photodiode arrray and a laser diode exhibits a gain ripple of ~1 dB over the entire bandwidth of 1.5 GHz. the noise floors of the two optical links exhibit same behaviours shown in Figure 4.19.b. These noise floors indicates that the overall noise of the optical link is dominated by the receiver noise as predicted in Chapter 2.

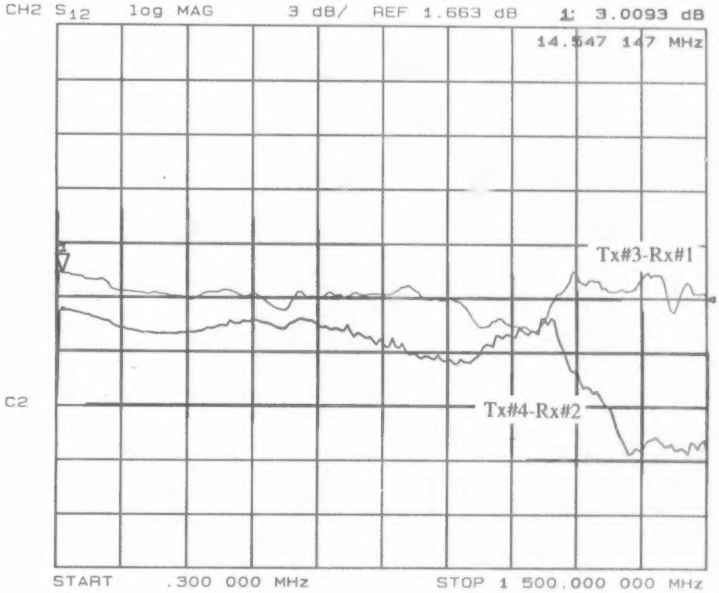


Figure 4.20 The frequency response of the two optical links. (a) Tx#3 and Rx#1 (b) Tx#4 and Rx#2

5.0 SYSTEM PERFORMANCE

A 2x2 switch matrix system, as shown in Figure 5.1, consisting of two transmitters and two receivers was assembled for demonstrating some of the proposed signal processing functions. The transmitters, receivers, and optical distribution system were designed for a 10x10 matrix which is to be completed in subsequent work.

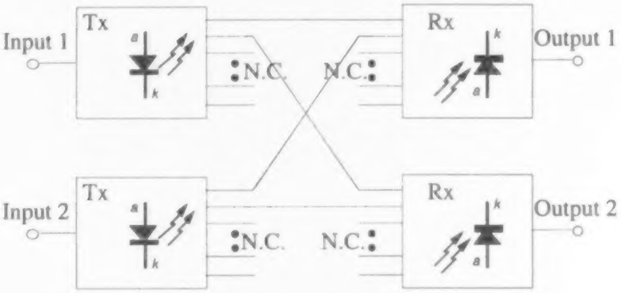


Figure 5.1 The 2x2 switch matrix system used for testing the signal processing functions

5.1 Crosspoint Characteristic

First, the switching parameters were measured in the 2x2 switch matrix. The isolation of a crosspoint was recorded at 1 GHz to be 50 dB by biasing the crosspoint at 5 V for ON and -15 mV[1] for OFF. Figures 5.2 and 5.3 shows the crosspoint isolation measurement recorded with a HP-8753A network analyzer and HP-71000 spectrum analyzer. Comparing Figures 5.2 and 5.3, it seems that the network analyzer measurement was not able to show the true isolation of the crosspoint. At the low frequency (300kHz - 10MHz) range, the network analyzer shows an isolation of 50 dB or more but in the high frequency (100MHz-2GHz) range, the isolation was degraded down to as low as 20 dB near 1 GHz. This low isolation is contrary to the observation with the spectrum analyzer measurement in Figure 5.3. This indicates that the high noise floor (-112 dBm) of the receiver affects the isolation measurement of the network analyzer at 1 GHz. This noise effect on the network analyzer should be noted for future isolation measurements.

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[1] This bias voltage varies from detector to detector.

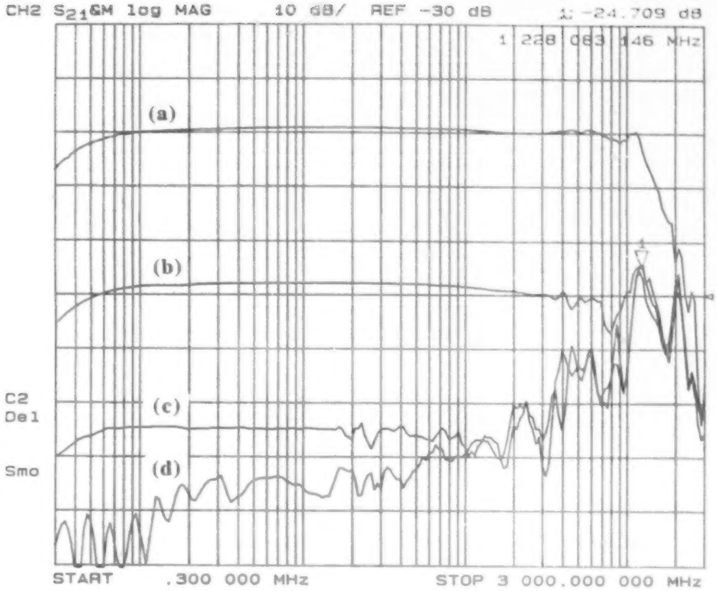


Figure 5.2 The crosspoint isolation measurement with a HP-8753A network analyzer. The bias conditions are (a) 5V, (b) 0V, (c) 12.7mV, and (d) open circuit.

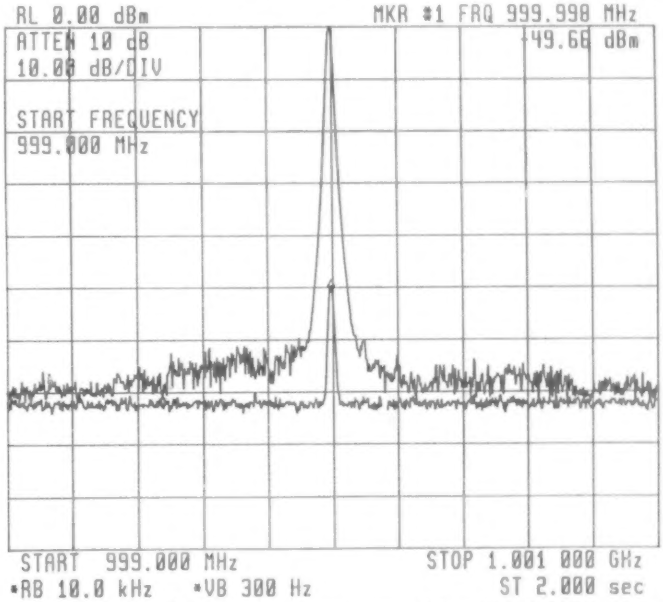
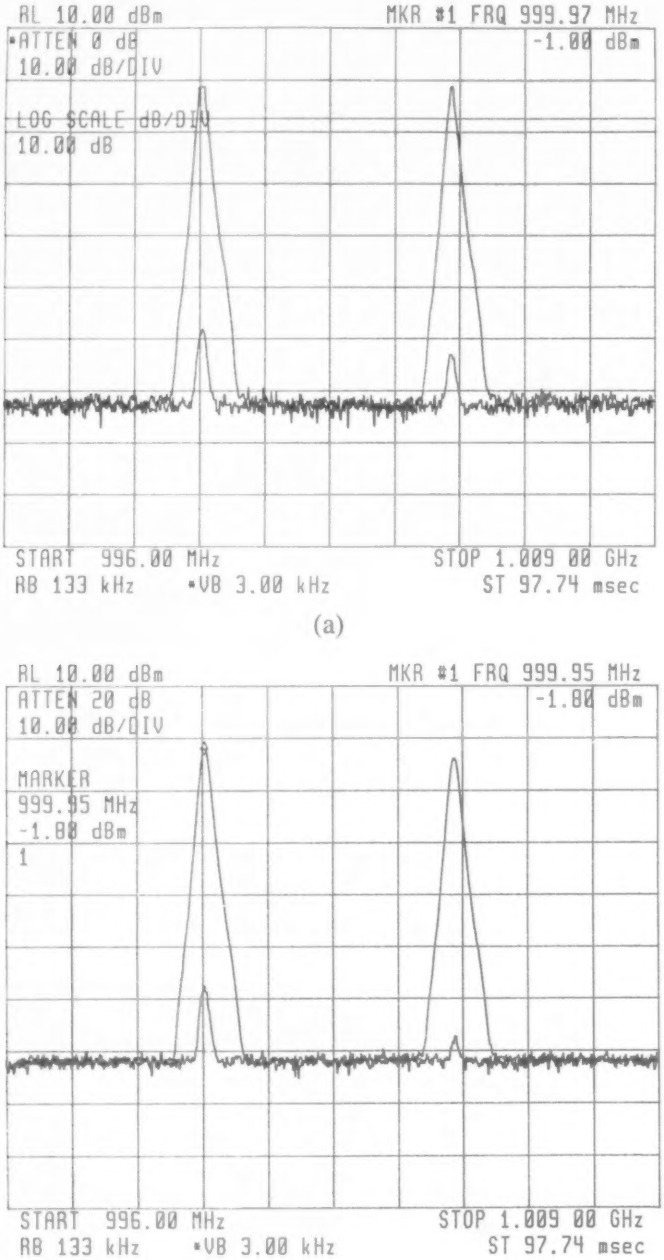


Figure 5.3 The crosspoint isolation measurement with a HP-8642A signal generator and a HP-7100 spectrum analyzer

Next, the optical cross-talk between two adjacent channels was investigated by illuminating two adjacent crosspoints with two optical signals modulated at different frequencies. The optical crosstalk was measured by biasing one crosspoint OFF and the other ON. Figure 5.4.a shows the spectra of the receiver output signal when crosspoints are biased both ON and both OFF; Figure 5.4.b shows the signal spectra for the two cases which only one crosspoint is biased ON. From Figure 5.4, the signal levels are



(a)

(b)

Figure 5.4 The optical cross-talk measurements. (a) the both crosspoints are biased at the same levels (ON or OFF). (b) only one crosspoint is biased ON.

dominated by the leakage from the OFF crosspoint and no optical cross-talk was observed between the adjacent channels; therefore, the optical cross-talk must be lower than the isolation of the crosspoint which is greater than 50 dB.

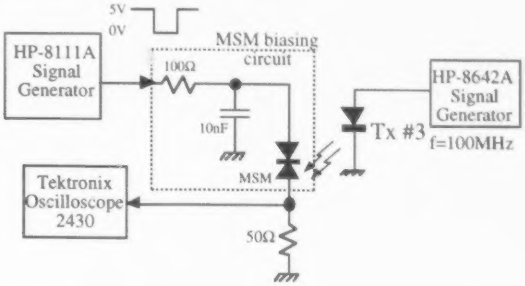
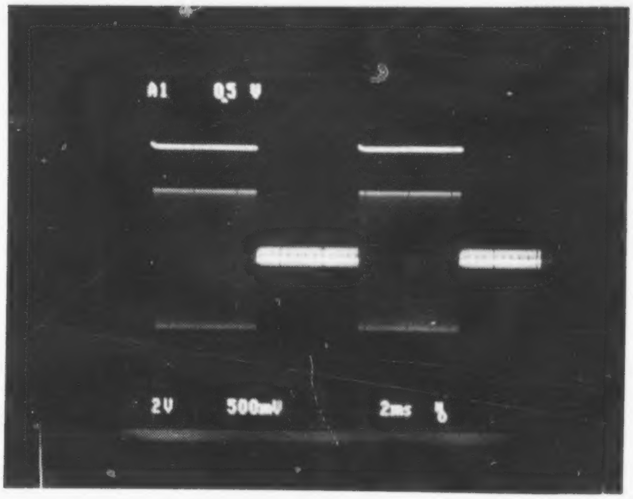
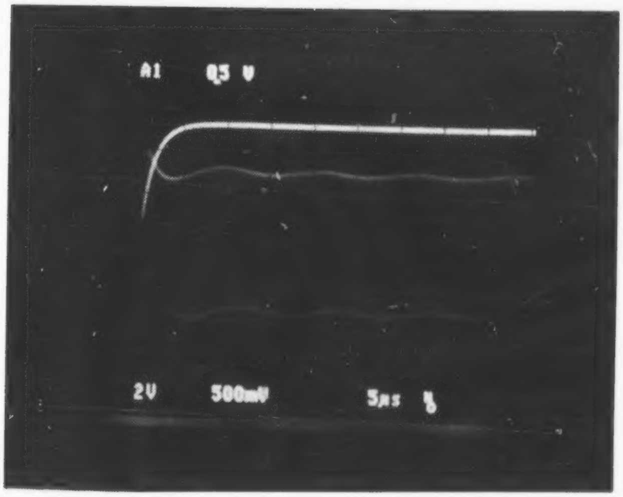

5V
0V
HP-8111A Signal Generator
MSM biasing circuit
100Ω
10nF
MSM
HP-8642A Signal Generator
Tx #3
f=100MHz
Tektronix Oscilloscope 2430
50Ω

Figure 5.5 The experimental setup for testing the switching characteristic of the MSM biasing circuit.

The switching characteristic of the MSM crosspoint with the biasing circuit was investigated with the experimental setup shown in Figure 5.5. The MSM biasing circuit was driven by a HP-8111A function generation with a rise time of less than 10 ns which is much less than the rise time of the proposed DAC output (~2.8 μs). Figure 5.6 shows that a 100 MHz sinusoidal output switched by biasing a voltage swinging from 5 to 0 volt at a repeat rate of 104 Hz. Both the rising and falling edges of the output signal exhibit a low level relaxation oscillation of approximate 20 kHz with an initial rise time of less than 1 μs and a settling time of 20 μs. The low frequency of the oscillation indicates that the oscillation might be caused by the relaxation of the amplifier power supply circuitry, rather than the MSM biasing circuit which is expected to oscillate at a much higher frequency. The rise and fall time of the MSM bias voltage is about 3 μs which is in agreement with the bias filter circuit time constant (RC ~ 1 μs). The rise time of the received output (~1 μs) is shorter than the rise time of the bias voltage. This discrepancy can be explained by the saturation of the MSM response at a lower voltage than the maximum applied.



(a)



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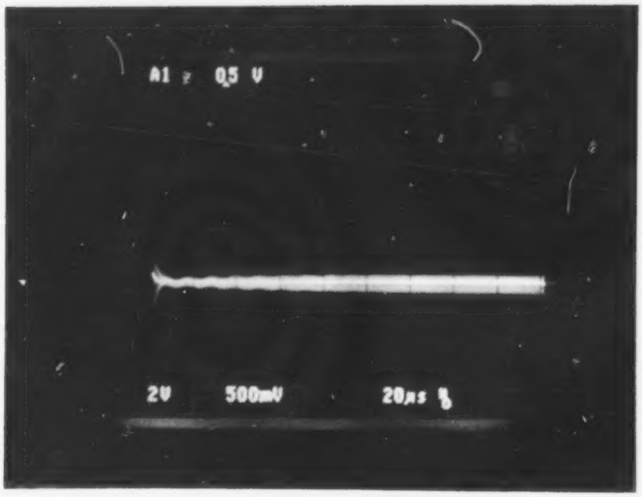


(c)
Figure 5.6 Switching transients measurements. (a) the bias voltage and the output signal, (b) the rising edges of the both signals, and (c) the falling edges of the both signals.

The switching time is much longer than the reported value of 100ns for a similar MSM photodiode [58]. Our switching time is mainly limited by the large capacitance required for bypassing the low frequency signal (~300kHz), rather than the intrinsic switching characteristic of the MSM photodiode. This capacitance limitation can be overcome by employing the high speed FET switch arrangement [58] in conjunction with the existing bias scheme. The proposed scheme shown Figure 5.7 can provide both the flexibility of continuous bias, and the capability of high speed switching. However, this scheme would also require doubling the complexity of the current system.

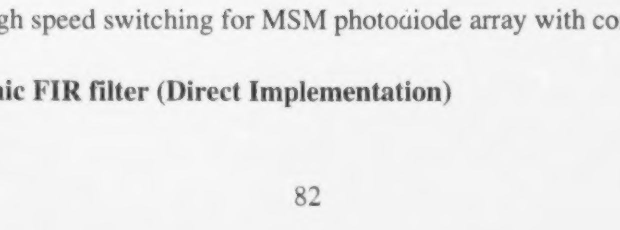


Figure 5.7 High speed switching for MSM photodiode array with continuous bias.

5.2 Optoelectronic FIR filter (Direct Implementation)

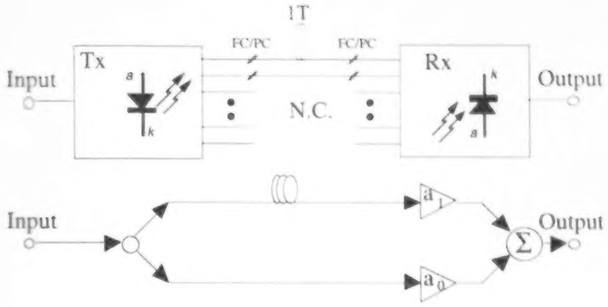
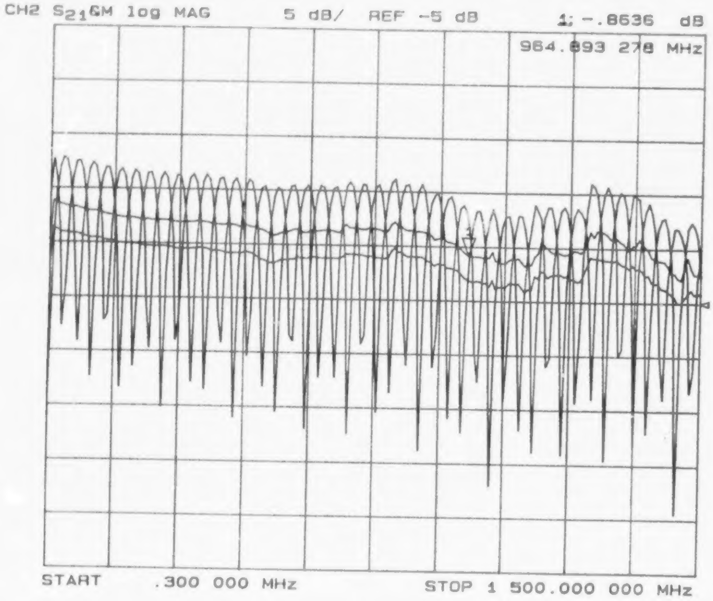


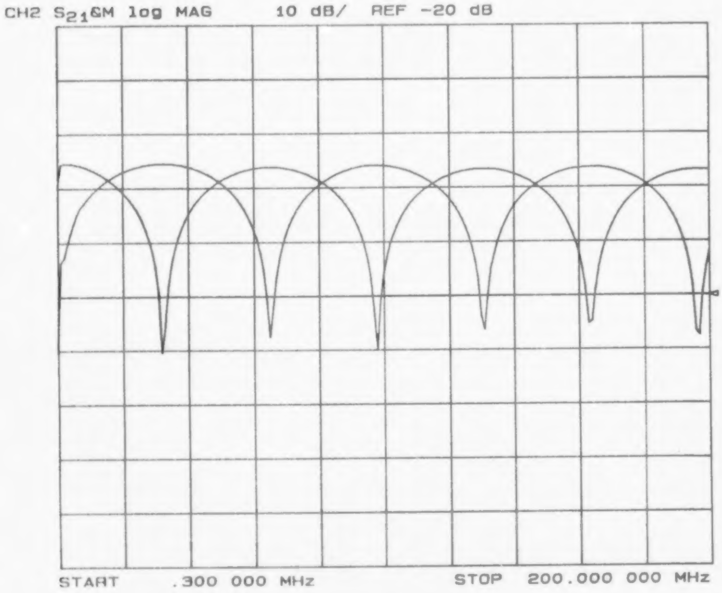
Figure 5.8 A block diagram of a 2-tap optoelectronic FIR filter using a direct implementation.

The optical backplane architecture allows the processor to have the flexibility to be configured into other forms than the square matrix form. For example, the system can be configured into 10 10-tap transversal filters by directly connecting each Tx-Rx pair with 10 differential delay lines in parallel. To demonstrate this filter form, the test system was configured into the 2-tap FIR filter shown Figure1.4 with an optical distribution and an optoelectronic summation. Figure 5.8 shows the connection of the system. Figure 5.9.a shows the responses of the system with delayed addition (Low pass response), delayed subtraction (High pass response), and the responses of each crosspoint under 5V bias over the entire bandwidth. Under a 5 V bias, the crosspoints differ in response by roughly 3 dB which is mainly caused by optical misalignments. This discrepancy between the crosspoint responses was simply overcome by lowering the bias of the higher response detector. After the bias compensation, a notch response of -35 dB was observed and recorded in Figure 5.9.b. The differential delay used is approximately equal to 15 ns (~3m in length) which corresponds to a fundamental frequency of 33 MHz. Figure 5.9.b and Figure 5.9.c show the detailed frequency responses of the high pass and low pass configurations at the two ends of the frequency spectrum. Note that the all-pass responses in Figure 5.9.c have a response difference of about 1 dB. This difference indicated that the responsivity of the two detectors over the frequency range has a slight difference in slope which might be caused by the different bias for the response compensation.

The signal spectrum of a 32 MHz signal under an all-pass response (i.e. only one crosspoint is ON) and a notch response was recorded in Figure 5.10. Note that the noise floor of the measurement is not affected by the filter response which indicating that the output noise is dominated by the receiver noise performance and the noise on the bias voltage discussed in Section 2.2.2.2 is not a significant factor in the noise performance of this FIR implementation.



(a)



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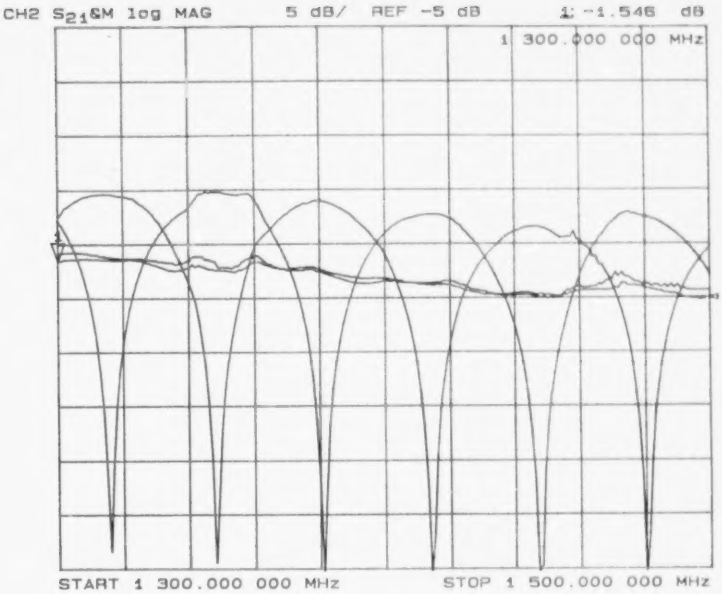


(c)

Figure 5.9 The direct implementation FIR filter responses. (a) The filter responses in a high-pass, in a low-pass, and in an all-pass (without bias compensation) configuration. (b) The high pass and low pass responses of (a) with bias compensation from 300 kHz to 200 MHz. (c) The frequency responses of (a) with bias compensation from1300 MHz to 1500 MHz.

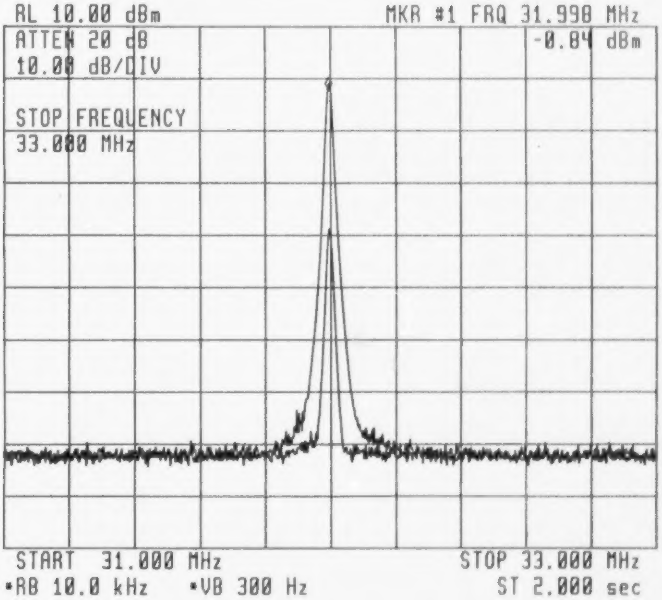
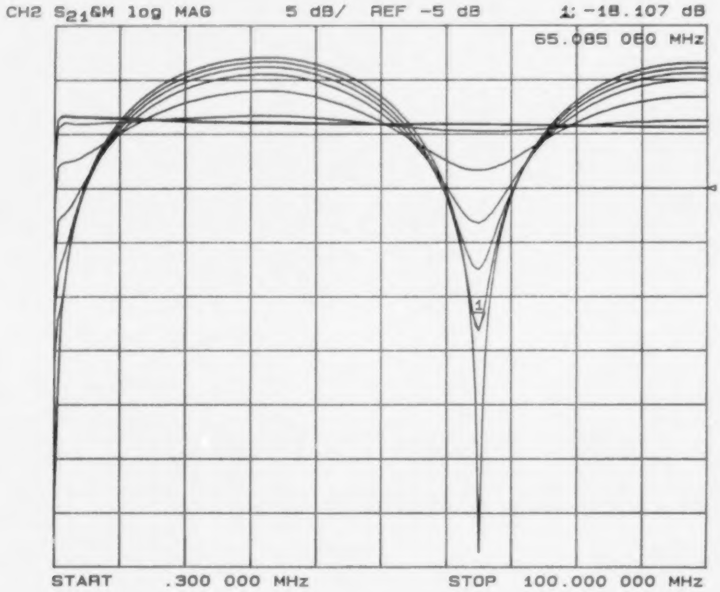
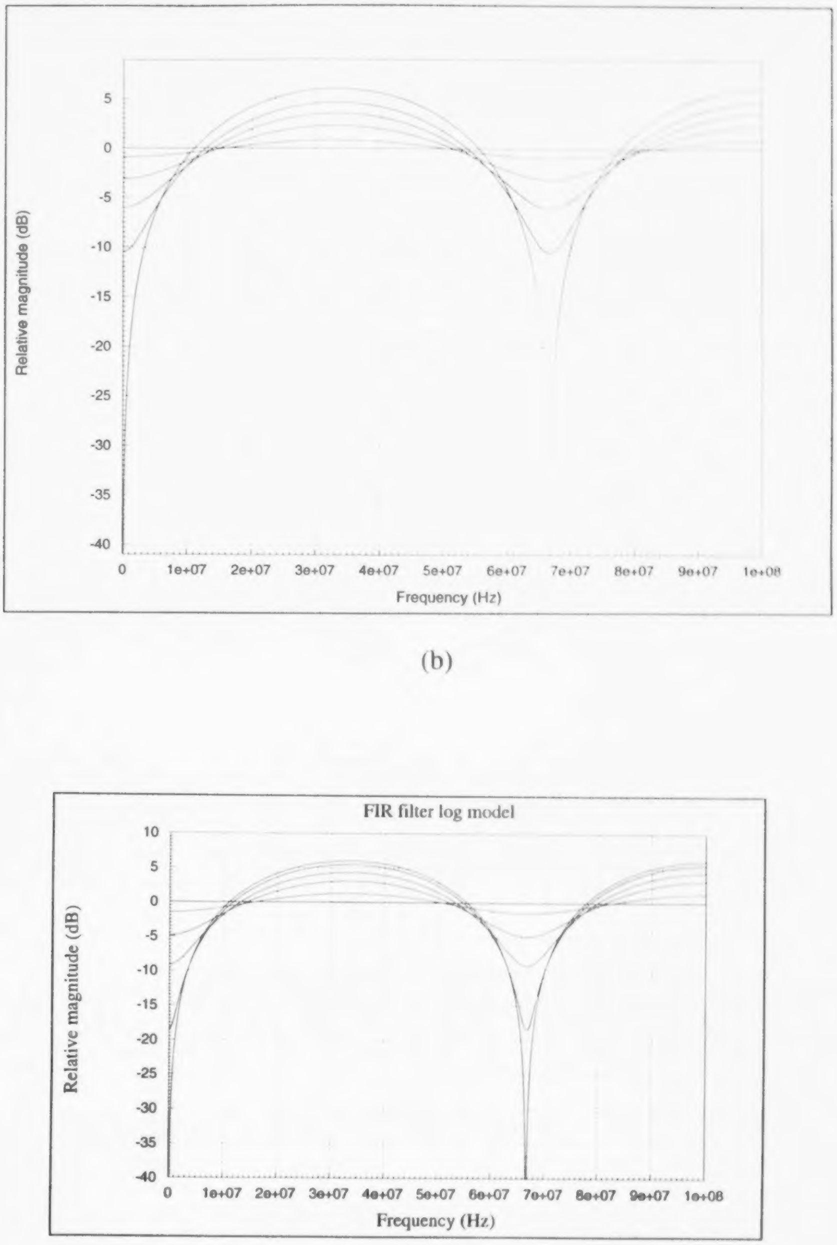


Figure 5.10 The spectrum measurement of a 32 MHz under both high pass and low pass response of FIR filter in Figure 5.8

Figure 5.11.a illustrates the frequency response of the low pass filter with different biases and Figure 5.11.b and 5.11.c are the calculated results of a 2 tap FIR filter using a linear model and a non-linear model for the responsivity-bias relationship. Based on a linear model, the peak value of the response is not matched well with the measurement value but the general bandpass shape is in agreement with the measured values. With a non-linear model based on the AC measurements in Figure 2.5 the calculated result is in agreement with the measured value. Therefore, the measured AC responsivity can be used to calibrate of the filter tap weights with the bias voltage.



(a)



(b)

(c)

Figure 5.11 The measured and predicted low pass response of the FIR filter response under different crosspoint biases. (a) the experimental results with one detector bias at 5V and the other detector biased at 1.25 V, 0.87V, 0.62V, 0.37V, 0.12V, 0V, and open circuit, (b) the calculated results based on a linear model, and (c) the calculateed results based on the measured responsivity.

5.3 Optoelectronic IIR Filter

Next, the test system is configured as one pole IIR filter (or a ring resonator) shown in Figure 5.11. An additional 10 dB attenuator is added to the signal path to protect the laser diode from the excessive drive from the receiver output. The maximum output of the receiver can be in excess of 5 V_p which is about 4 times greater than the damaging drive voltage of the laser diode (~1.25 V_p). This attenuation severely degrades the possible quality factor (Q) of this IIR filter design. In future implementations, a high speed limiting diode should be added to limit the maximum input power of the transmitter.

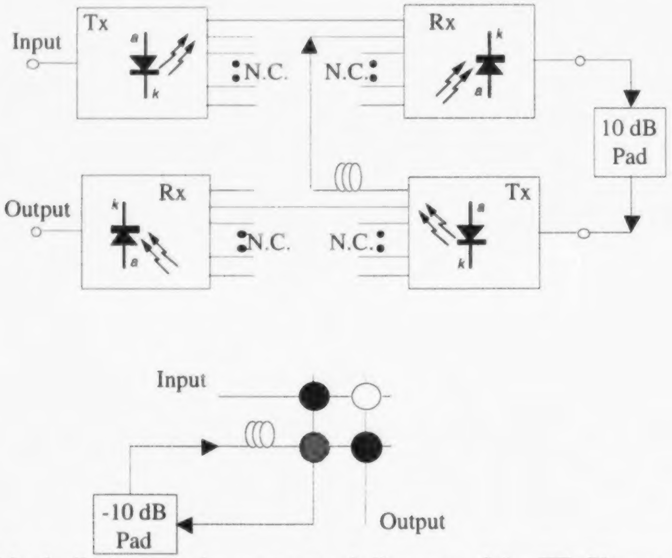


Figure 5.12 A block diagram and a conceptual diagram of the IIR filter using the 2x2 test system

Figure 5.13 shows the frequency response over 1.5 GHz of the IIR filter with a +/- 5 V bias on the feedback crosspoint. The reflex time is calculated to be 18 ns based on the resonant frequency period. The peak to peak difference in filter response is about 5 ~ 6 dB over the entire bandwidth, which is in agreement with the predicted value of 5.6 dB. Figure 5.14 shows the frequency response and the noise floor of the filter from 500 MHz to 700 MHz. Notice that the noise floor has approximately 1 dB ripple which is caused by the noise enhancement effect discussed in Section 2.2.2.3. Based on a modified version of Eq. 2.20 accounting for the 10 dB attenuation, the upper bound on noise peaks for the ring resonator should be 1.1 times original noise power. With the output receiver noise, the predicted upper bound noise increase is 2.6 dB which is greater than the 1dB peak observed. An analytical noise calculation based on additive noise sources predictes the peak-to-peak value of the noise floor to be 0.7 dB which matches the measured ripple value of roughly 1 dB.

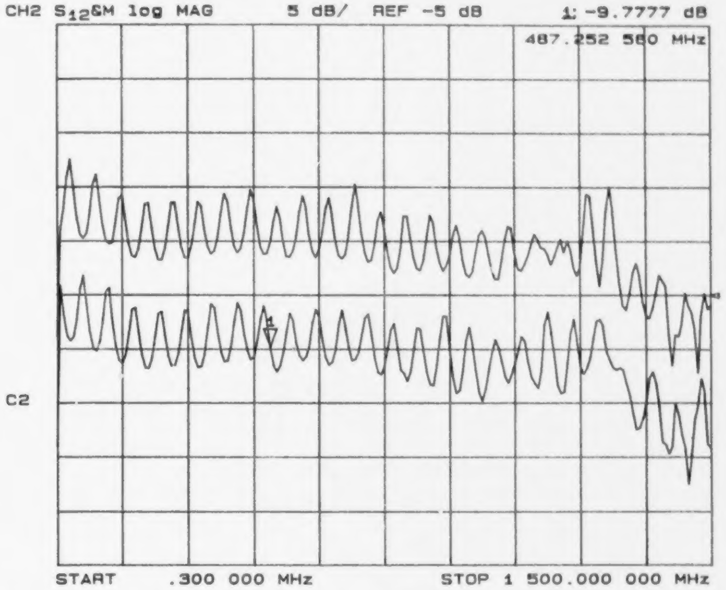
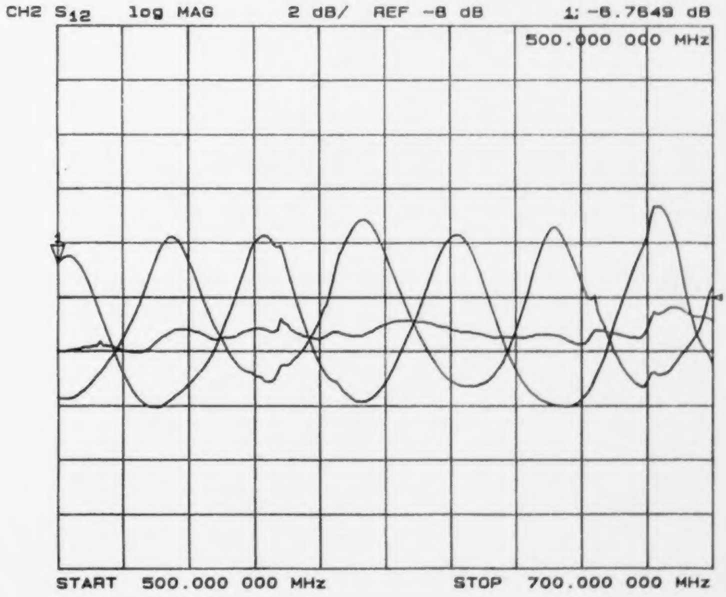
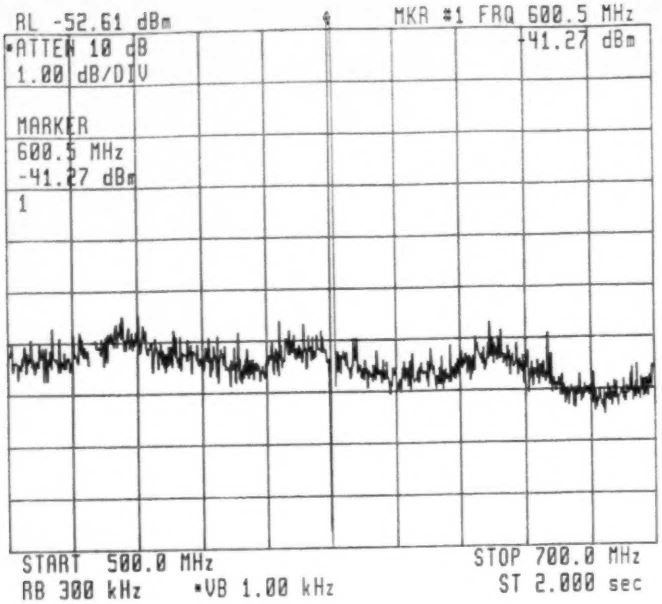


Figure 5.13 The frequency response of the IIR filter over a 1.5 GHz with positive and negative weights. Note the low curve is offset by -10 dB.



(a)

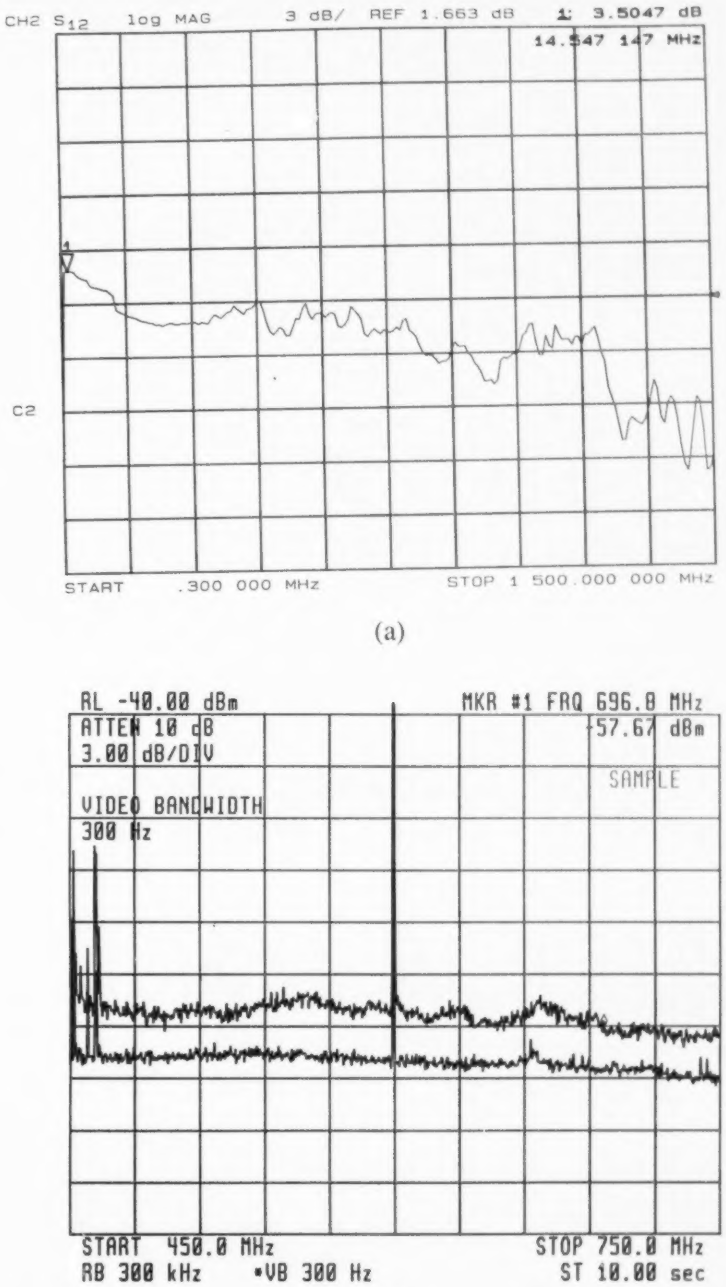


(b)

Figure 5.14 (a) The frequency response and (b) noise floor measurement of the IIR filter from 500 MHz to 700 MHz

5.4 Cascading Switches

The effect of cascading switches was studied with the configuration shown in Figure 2.7. A two stage cascading system was tested with the 2x2 switch. First, the noise floor and frequency response of the cascading stages are measured and recorded in Figure 5.15. From Figure 5.15.a, the noise floor of the cascading stages is approximately 3 dB above the single stage case. This 3 dB noise increase seems to indicate that the cascading noise has an additive behavior, but this study is not conclusive due to the limited number of available Tx-Rx pairs. The ripples on the noise floor of the system are chiefly due to the frequency response of the cascading system which is shown in Figure 5.15.b. The 3dB bandwidth of the cascading system is roughly 900 MHz with +/- 1.5 dB gain ripple. The cascaded bandwidth reduction is not too severe (~400 MHz lower than a single stage) but the large gain ripple seems to be a more important limiting factor on the number of cascading stages. The large gain ripples may be solved by better matching between the gain stage and reducing cable length between transmitters and receivers to minimize the electrical reflections.



(a)

(b)

Figure 5.15 The noise floor and the frequency response of the two cascading stages. (a) The top trace is the two cascading stages and the bottom trace is the noise floor of the first stage. The noise peak at 450 MHz is caused by radio interference. (b) The frequency response of the cascading stages.

5.5 Optoelectronic FIR Filter (Reflex Implementation)

Finally, an attempt to test the reflex implementation of the FIR filter was made. Implementing the reflex FIR filter shown Figure 2.8.a would require a minimum of 3 Tx-Rx pairs. Due to a shortage of Tx-Rx's, the first stage optoelectronic signal distribution is replaced with an electrical distribution which consists of a 1-to-2 electrical power splitter. The effect of the additional optoelectronic distribution stage can be estimated by examining the results from Section 5.4. From Section 5.4, the major impairments of the cascading stages are on the noise floor and the gain ripple. The noise floor does not greatly affect the filter performance but the large gain ripple is expected to distort the overall reflex FIR filter response.

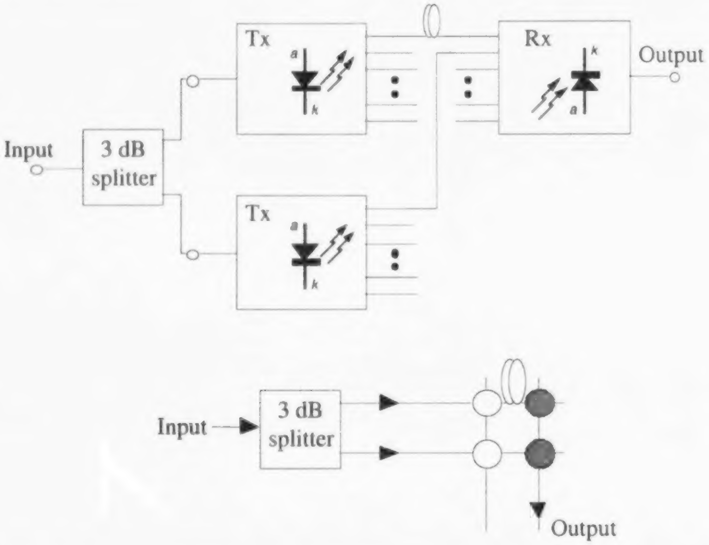
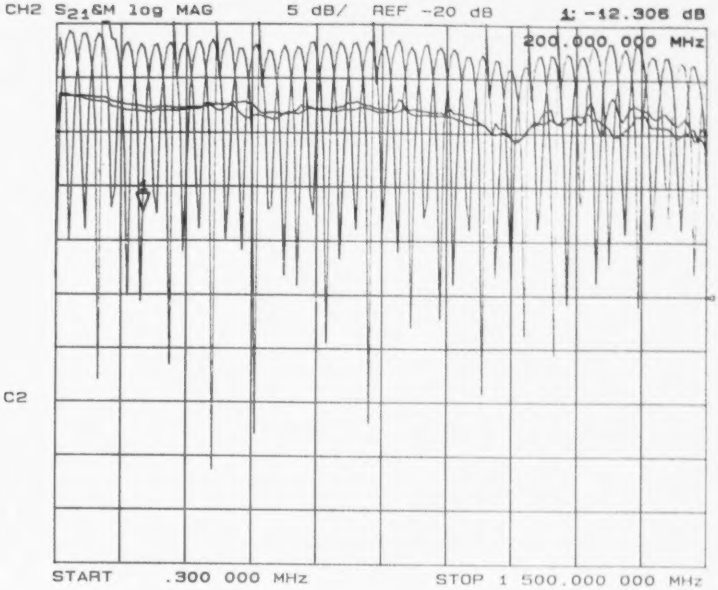
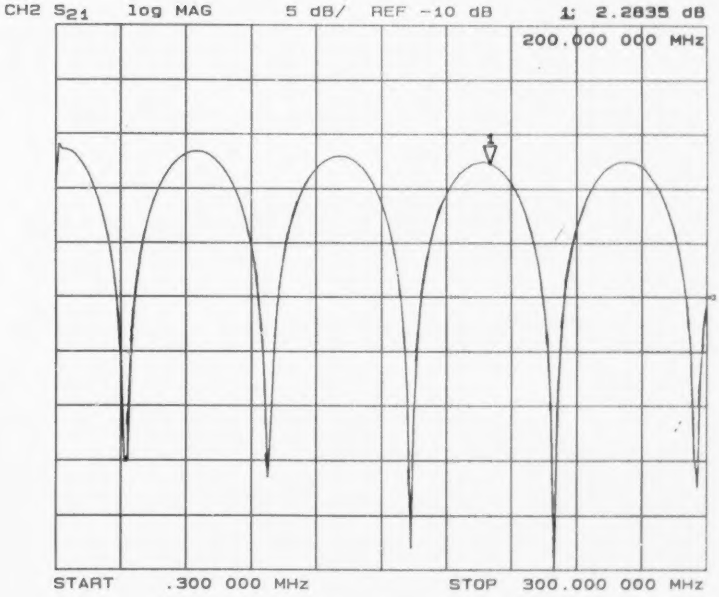


Figure 5.16 A block diagram and a conceptual diagram of the reflex FIR filter using the 2x2 test system

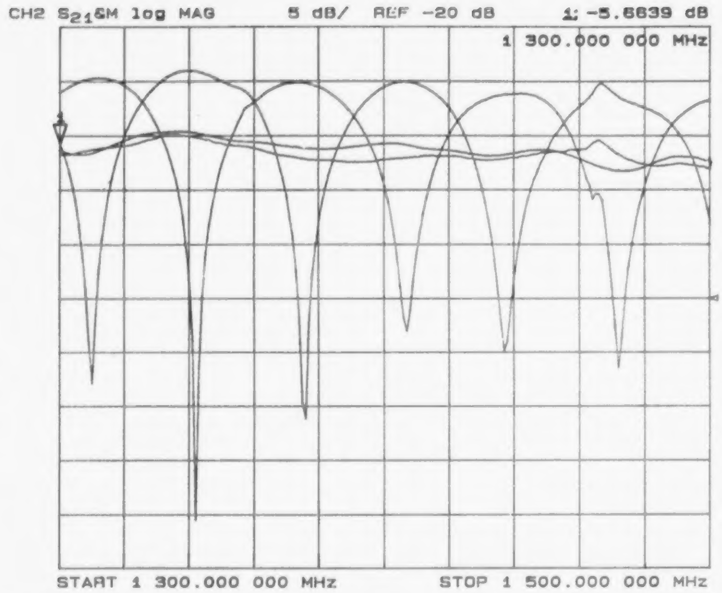
Figure 5.16 shows the block diagram of the modified reflex FIR filter. The responses of the two paths are within 0.5 dB which is an improvement over the response from Section 5.2; this improvement is a result of an improved optical alignment. The high pass and low-pass are similar to the results from Section 5.2. Figure 5.17 shows the frequency response of the FIR filter with a differential delay of 15 ns. Note that there are some spurious peaks in Figure 5.17.a. These peaks are believed to be an artifact of the measurement. These peaks vanish from the measurements when the scanning frequency range is reduced from 1.5 GHz to 200 MHz. Again, the noise floor of the system is not affected by the filter response or the crosspoint setting. The noise is still dominated by the receiver thermal noise.


CH2 S21&M log MAG
5 dB/ REF -20 dB
1: -12.306 dB
200.000 000 MHz
C2
START .300 000 MHz
STOP 1 500.000 000 MHz

(a)


CH2 S21 log MAG
5 dB/ REF -10 dB
1: 2.2835 dB
200.000 000 MHz
START .300 000 MHz
STOP 300.000 000 MHz

(b)



(c)

Figure 5.17 The high pass, low pass, and all pass responses of the reflex FIR filter (a) over 1.5 GHz, (b) from 300 kHz to 200 MHz, and (c) 1300 MHz to 1500 MHz.

In general, the response obtained by using two different transmitters to generate optical signals has no significant difference from the results generated by using one transmitter. A slightly higher gain ripple was observed on the overall gain flatness which may be caused by the difference in response between the two transmitters. The responses are expected to be degraded severely for the reflex FIR filter because of the large gain ripples observed from the cascading stages in Section 5.4.

6.0 SUMMARY

In this thesis, two main subjects were discussed. First, the design and construction of a signal processor using an optoelectronic switch matrix and replaceable optical fiber delay lines was presented. Second, signal processing applications of this processor were demonstrated. In this chapter, the primary results of this thesis are summarized and a brief discussion of future work is presented.

6.1 The Optoelectronic Signal Processor

The proposed optoelectronic signal processor consists of a 10x10 optoelectronic switch matrix and 10 replaceable optical fiber delay lines. The overall processor is organized into transmitter and receiver modules. These modules are connected together via an optical backplane housed at the back of the transmitter module. This backplane allows different processor configurations other than the square matrix form.

The transmitter module is organized into 10 transmitter cards. Each transmitter card houses a laser diode, an optical power distribution network and an optical fiber delay line. Ten transmitter circuit cards were built and tested. The modulation bandwidths of these transmitters were measured and varied from 1.1 to 1.6 GHz. The dynamic range of a transmitter was recorded up to -131 dB/Hz. A low frequency fluctuation of the AC output level was observed at +/- 0.25 dB over a 30 second period. The uniformity of the optical outputs were measured within +/-0.04 mW (+/-10%) over 10 outputs. The optical insertion losses of the complete optical distribution network were recorded at 11.2 +/- 0.5 dB.

The receiver module is also organized into 10 receiver cards. Each receiver card consists of 10 programmable voltage sources for biasing each photodiode in a metal-semiconductor-metal (MSM) photodiode array and a MSM optical receiver for performing the optoelectronic conversion. An additional microcontroller card is added to allow the external world to program the biasing sources. Functionally, the receiver module is divided into two subsystems: MSM biasing system and MSM optical receiver. The MSM bias system generates the control voltages for performing the optoelectronic weight setting function; the MSM optical receiver performs the optoelectronic conversion and compensates for the link losses.

The MSM bias system is made up of a microcontroller card and 100 independently addressed 12-bit DAC's. The MSM bias system was successfully built and tested. The system provides a 100 programmable voltage sources with a range of +/-5V and a 4 mV resolution for controlling the responsivities of the 100 MSM photodiode crosspoints. 6 mV_p voltage spikes were observed on the voltage outputs during the switching transition. These spikes are expected to be removed from the bias voltage by the biasing filter on the MSM optical receiver circuit. The rise times for these voltage source are measured at about 2.8 μs for a full scale (10V) voltage swing. These rise times are too slow for high speed switching application but sufficient for most signal processing applications.

Ten MSM optical receivers were originally planned for the processor. The original optical receiver design experiences both stability and a unexpectedly low bandwidth problems. After further investigation, the stability problem was found to originate from the poor quality of the amplifier circuit board; the low bandwidth was caused by the high aggregate MSM detector capacitance. These problems were temporarily solved by modifying the amplifier design. The two modified amplifiers with a gain of 56 dB were tested to have bandwidths of 1.7 and 1.6 GHz with +/-1 dB gain ripple and a noise floor of -112 dBm/Hz. The overall performance of the optical receiver with optical input from the transmitter module were measured with bandwidths of 1.2 GHz and 1.3 GHz, and noise floors of -112 dBm/Hz.

6.2 System Performance

Based on the two optical receivers and transmitters, a 2x2 switch matrix was assembled for testing different signal processing functions. First, the switching characteristics of the crosspoints were tested. The isolation of the crosspoints, and the optical crosstalk between the adjacent channels were less than -50 dB. The switching time of the crosspoint was tested to be about 1 μs and was limited by the biasing circuit rather than the detector speed.

Next, the network was configured into three different filter forms: a direct implementation FIR filter, an IIR filter, and a reflex FIR filter. The frequency response and the noise behavior of these filters, were in agreement with the theoretical predictions. Demonstrations of manipulating and calibrating the filter response with the bias voltage were also conducted.

Finally, the effects of cascading stages on the system performance were investigated. The noise of the multistage network seems to exhibit an additive behavior but the study was not conclusive due to insufficient number of stages. A more serious impairment of a cascading network seems to be the electrical mismatching which causes a high gain ripple on the overall system response. This gain ripple must be eliminated before any large scale multistage network can be implemented.

6.3 Future Research Directions

As a consequence of this project, the following areas have been identified for future efforts:

1. The improved design amplifier must be designed with more stability and improved matching characteristics and manufactured with more consistency. This would allow the demonstration and large scale multistage system.
2. complete the overall system.
3. Once the larger system is completed, the effort should be focused on the study of the adaptive signal processing with the processor. The time fluctuation of the system gain could be a limiting factor on the adaptive system performance.

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APPENDIX A THE REQUIRED GAIN CALCULATION FOR THE MSM OPTICAL RECEIVER AMPLIFIER

In this section the expected signal level and the required power gain for the receiver are determined.

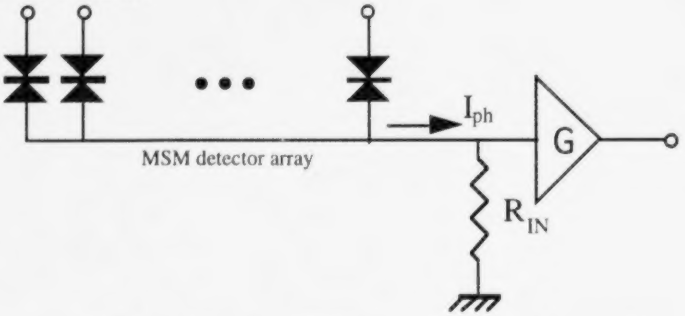


Figure A.1 The input circuit of the MSM receiver

Figure A.1 shows the equivalent circuit for the MSM front end stage with a common load. The photocurrent of the MSM array is given by

$$I_{Ph(p)} = R_{MSM}(\overline{P}_o)(MI)(IL)\sqrt{N} \tag{A.1}$$

where $I_{ph(p)}$ is the peak photocurrent, R is the responsivity of the detectors, P_o is the average optical power from a laser, MI is the modulation index of the intensity modulated signal, and N is the number of fully ON detectors on the array. The number of fully ON detectors is dependent on the application. For example, only one detector is turned ON at a time in a switching application; on the other hand, for an optoelectronic weight setting and summation application more than one detector is sensitized at a time. For most filter designs with an unity bandpass gain, the sum of the tap weights is equal to or less than one. We assume that only one detector is fully on at any given instant. Based on N=1, the maximum peak photocurrent, $I_{ph(max)}$, is given by

$$I_{ph(\max)} = R_{MSM}\overline{P}_o IL \tag{A.2}$$

The AC responsivities of the photodiodes range from 0.16 to 0.2 A/W which are typical of the tested samples. The average optical power is about 5 mW. The insertion loss of a typical optical path is assumed to be 15 dB which consists of 13 dB splitter loss and 2 dB excessive loss on the splices. Based on these values, the peak photocurrent is found to be $I_{ph(MAX)} = 2.53 * 10^{-5} \leftrightarrow 3.16 * 10^{-5}\ A_p$. The input electrical power of the receiver amplifier is given by

$$P_{in(MAX)} = \frac{I^2_{ph(MAX)} R_{in(eq)}}{2} \tag{A.3}$$

where R_{in}(eq) is the equivalent input impedance of the receiver amplifier. Assuming an input resistance of 50 ohms, the maximum input power is 16.0 <=> 25.0 n W. The expected output level of the receiver is about 10 dBm which satisfies the requirement for a 100% modulation index for the laser of the next stage. With a maximum input power of 16.0 <=> 25.0 nW and a maximum output power of 10 dBm, the required gain is estimated about 58 <==> 56 dB. The overall gain is set to be 60 dB for the receiver amplifiers.

APPENDIX B: IMPAIRMENTS OF MULTISTAGE OPTOELECTRONIC SWITCH NETWORKS

When an optoelectronic (o/e) switch network uses multiple cascading stages, the signals suffer from additional signal degradation. This degradation will determine the number of stages that can be cascaded before the signals require regeneration (in digital form) or are rendered useless (in analog form). The major sources of the degradation caused by cascading the o/e matrix are individual stage bandwidth reduction, noise accumulation, and cross channel interference from non-ideal crosspoints and also electromagnetic crosstalk coupling. In the following section, the effects of these factors are discussed and analyzed.

In the following analysis, we assume that the individual stage can be modeled by a linear time invariant first order low pass filter and that the noise sources in the system are additive in nature. The frequency response of each stage, H(f) is described by

$$H(f) = \frac{H_0}{(1 + jf / f_c)} \tag{B.1}$$

where H_O is the DC response of a stage, f_c is the 3dB corner frequency of the individual stage, and f is the operating frequency.

First, we consider the effects of bandwidth reduction due to cascading stages. Since the system is first order and linear time invariant, the response of multiple stage can be represented as

$$H_N(f) = \prod_{i=1}^{N} H_i(f) \tag{B.2}$$

where $H_i(f)$ is the frequency response of each individual stage and N is the number of stages. Assuming all stages are identical, Eq.(B.2) can be rewritten as

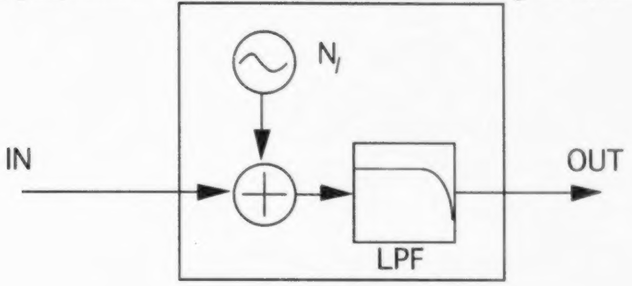
$$H_N(f) = \left[\frac{H_o}{(1 + jf / f_c)} \right]^N \tag{B.3}$$

The 3dB corner frequency of the overall network, f_c' can be determined by solving

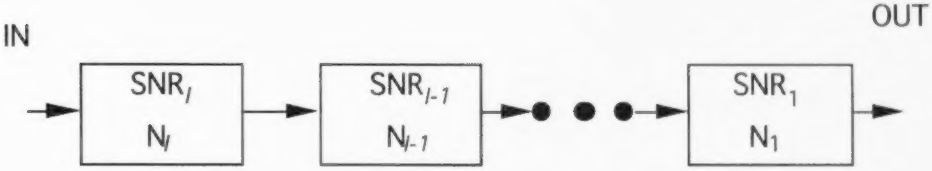
$$\left| H_N(f_c') \right|^2 = 0.5 * \left| H_N(0) \right|^2 \quad . \tag{B.4}$$

The effect of cascading stages is to increase the order of the system to N. The 3 dB corner frequency of the overall network is reduced by a factor of $\frac{1}{\sqrt{\sqrt[N]{2} - 1}}$ or the 3db corner frequency of an individual stage must be expanded by a factor of $\frac{1}{\sqrt{\sqrt[N]{2}-1}}$ in order to maintain the same corner frequency. This bandwidth reduction will have an impact on the noise performance of the system.

The noise effect from the cascading stages can be analyzed as a series of noisy first order low pass filters. Figure B.1 shows the block diagram of this model.



Single stage noise model



Multistage noise model

Figure B.1 Noise models of a single stage and cascading stages

Each stage consists of a noise source cascaded by a low pass filter with a corner frequency, f_c. In general, the signal-to-noise ratio (SNR) of a multiple identical stage system with unity gain is given as

$$SNR_m = {SNR_s}/{N} \tag{B.5}$$

where SNR_m is the SNR of the overall network, SNR_s is the signal-to-noise ratio of a single stage, and N is the number of stages. If we account for the low pass effect of each stage, the SNR of a multiple identical stage network can be written as

$$SNR_m = \frac{1}{\sum_{i=1}^{N} \frac{1}{SNR_i / K_i}} \tag{B.6}$$

where SNR_i is the SNR of the i^{th} stage and K_i is the noise bandwidth reduction factor. For each stage, the SNR is determined by

$$SNR = \frac{S_{\max}}{N_o} \tag{B.7}$$

where $S_{\max}$ is the maximum available signal power and N_O is the noise power which is given by:

$$N_o = \int_{-\infty}^{\infty} \frac{S_n}{\left[1+\left(f/f_c\right)^2\right]} df \tag{B.8}$$

where S_n is the noise power spectral density of the noisy source. Since the noise of the pervious stage is treated as signal in the subsequent stages, N_o is reduced by the low pass filter action of subsequent stages. This reduction is given by

$$K_i = \frac{\int_{-\infty}^{\infty} \left[\frac{1}{1+\left(f/f_c\right)^2}\right]^i df}{\int_{-\infty}^{\infty} \frac{1}{1+\left(f/f_c\right)^2} df} \tag{B.9}$$

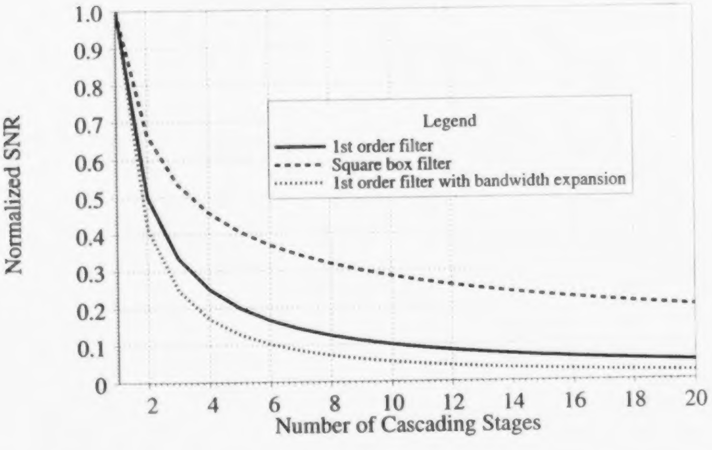


Figure B.2 The SNR behaviors as a function of number cascading stages

Figure B.2 shows the effects of cascading a number of model stages with three different output filters. The first case, we assume the output filter is modeled with a square box filter; therefore, the bandwidth reduction factor is always 1 and the overall SNR is behaved according to Eq.B.5. In second case, the model stages are simply connected in series. The SNR is decreased slower than the first case because the noise bandwidth is reduced by the factor of $\frac{1}{\sqrt{\sqrt[N]{2}-1}}$ as the number of stages increases; however, the signal bandwidth is reduced by the same factor as a result. The third case shows the SNR behavior with an extended bandwidth to compensate the bandwidth reduced due to cascading stages. In this case, the SNR is decreased rapidly as the number of stages increases.

Another source of signal degradation for the multistage network is the crosstalk between channels. The crosstalk in each stage can be estimated by

$$CP = ER * S_{\max} * (n-1) \tag{B.9}$$

where CP is the crosstalk signal power, ER is the extinct ratio of each crosspoint, and n is the dimension of a single stage. Since crosstalk is simply an undesired signal, the noise bandwidth expansion has no effect on crosstalk and the cumulative crosstalk for a N stage network is simply the N times the single stage crosstalk

$$CP_a = CP * N \tag{B.10}$$

However, if we consider the fact that the multistage network can reduce the dimension of the individual stages, the effect of cumulative crosstalk can actually result in an improvement over a single large network. For example, a 100X100 single network generates a crosstalk of ER*$S_{\max}$*99. On the other hand, a 3 stage Clos network with 30 10X10 sub-matrices generates a crosstalk of ER*$S_{\max}$*27, which is ≈ 3 times improvement over the single large network. This improvement is dependent on the extinction ratio of each crosspoint and the structure of the network.

The effect of multistage o/e switch networks on the performance of the system was examined. Cascading switch matrix requires the bandwidth of each individual stage to expaned its bandwidth to maintain the same system bandwidth. Based on a first order model, this bandwidth expansion factor is found to be $\frac{1}{\sqrt{\sqrt[N]{2}-1}}$. For higher order systems, similar noise bandwidth expansion can be observed but with a different expansion factor. The noise performance of a multistage network suffers in twofold: (1)

noise accumulation through stages and (2) noise bandwidth expansion. Finally, the effect of crosstalk in a multistage system was studied. The multistage system seems to have an advantage over a large single stage system in term of crosstalk performance. The combined effect of a multistage network is dependent on the network structure as well as the crosspoints involved.

APPENDIX C SIMULATION MODEL FOR THE SYSTEM PARAMETER VARIATIONS

This appendix contains two simulation programs for modeling the effects of delay time and Tx-Rx pair frequency response variations on a 20 tap FIR bandpass filter. The first program simulates the effect of the Tx-Rx pair frequency response. The frequency response variations are modeled by a simple multiple pole low pass filter with random frequency response. This program consists of five files: complex.c, complex.h, main.c, model.c, and model.h. Complex.c and complex.h are the complex number library for the program. model.c and model.h contains the routines for calculating the filter weight and for simulating the random fluctuation of the Rx-Tx. main.c contains the main routine of the program. First, the program reads the simulation parameters, such as bandpass filter and order of the response, from the console and passes these parameter to model.c for setting up the model. Then the program repeatedly calls model.c to calculate the FIR bandpass response. The frequency response of the model is randomly fluctuated according to the setup parameters. Finally, the statistic of the output response is gathered and printed out on the console.

The following are the listing of the frequency response variation program:

Listing C.1 main.c (for Tx-Rx pair frequency response simulation)

```
#include <stdio.h>
#include <math.h>
#include "complex.h"
#include "model.h"

#define Span 1.0
#define Lower_freq 1.0
#define Order 5
#define Lower_corner 0.2
#define Upper_corner 0.4
#define Coarse 5
#define Fine 5

double pi;

main()
{
                complex resp;
                double mean[Num_Samples];
                double var[Num_Samples];
                void read_data();
                void srand48();

                int i, j, n, m;
                double f, df, tmp;
                double tmp1,drand48();
                double span, lf, lc, uc;
                int ci, fi;
                long seed;

                pi = 4.0 * atan(1.0);


                read_data(&span, &lf, &i, &lc, &uc, &ci, &fi, &seed);
                srand48(seed);

                printf("rx_tx spec:  span=%e\n", span);
                printf("            lower_freq=%e\n", lf);
                printf("            order=%i\n",i);
                printf("filter spec: lower corner=%e\n", lc);
                printf("            upper corner=%e\n", uc);
                printf("            fine increments=%i\n", fi);
```

```
        printf("        coarse increments=%i\n", ci);
        printf("        seed for random generator = %i \n", seed);

        init_tx_rx(span, lf, i);
        filter_init(lc, uc, ci, fi);
        init_stat(mean, var, Num_Samples);
        df = 1.0/2.0/Num_Samples;

        for (i=0; i!=Num_Runs; i++)
        {
                new_filter();
                f = 0.0;
                for (j=0; j!=Num_Samples; j++)
                {
                        f_resp(f, &resp);
                        tmp = sqrt(resp.r*resp.r + resp.i*resp.i);
                        update_stat(tmp, mean, var, j);
                        f += df;
                };
        };
/*
printf("Calc average\n");
*/
        get_stat(mean, var, Num_Runs, Num_Samples);
/*
printf("Done \n");
*/
        f = 0.0;
        printf("freq\t\t\t\tupper\t\t\tlower\t\t\tideal\n");
        for (i=0;i!=Num_Samples; i++)
        {
                printf("%e\t",f);
                printf("%e\t%e\t%e\n", mean[i]+var[i], fabs(mean[i]-var[i]), ideal(f));
                f += df;
        };
}
void read_data(span, lf, i, lc, uc, ci, fi, seed)
double *span, *lf, *lc, *uc;
int *ci, *fi, *i;
long *seed;
{
        printf("Frequency span = ");
        scanf("%le", span);
        printf("Lower frequency = ");
        scanf("%le", lf);
        printf("Order = ");
        scanf("%i", i);
        printf("Lower frequency corner = ");
        scanf("%le", lc);
        printf("Upper frequency corner =");
        scanf("%le", uc);
        printf("Coarse increments = ");
        scanf("%i", ci);
        printf("Fine increments = ");
        scanf("%i", fi);
        printf("Random generator seed = ");
        scanf("%li", seed);
}
```

Listing C.2 model.c (for Tx-Rx pair frequency response simulation)

```
#include <math.h>
#include <stdio.h>
#include "complex.h"
#include "model.h"

extern double pi;

static double weight[Max_Coarse * Max_Fine] = {0.0};
static double e_delay [Max_Fine] = {0.0};
static double o_delay [Max_Coarse] = {0.0};

static int f_init=0;
static double DT;
static int Coarse = 10;
static int Fine = 10;

void bandpass (lower, upper, taps, weights)
double lower;
double upper;
int taps;
double weights[];
{
        int i;

        printf("bandpass %e %e %i\n", lower, upper, taps);

        for (i=0; i!=taps/2 + 1; i++)
        {
                if (i == 0)
                {
                        weights[taps/2] = (upper - lower) / 0.5;
                } else {
                        weights[taps/2 - i] = weights[taps/2 + i] =
                        1.0/pi/i*(sin(2.0*i*upper*pi) - sin(2.0*i*lower*pi));
                }
        }
        for (i=0;i!=taps;i++)
                        printf("%i %e\n", i, weights[i]);

}

void f_resp(f, resp)
double f;
complex *resp;
{
        void o_del_resp();
        void e_del_resp();
        void tx_rx();
        void filter_init();

        complex resp1, resp2, tmp;
        complex o_resp[10], e_resp[10];
        int i, j;

        if (f_init == 0)
                {
                printf("auto_init()\n");
                filter_init(0.1, 0.25, 10,10);
                }

        for (i=0;i!=Coarse;i++)
        {
                o_del_resp(f,i, &o_resp[i]);
        }
        for (i=0;i!=Fine;i++)
        {
                e_del_resp(f,i,&e_resp[i]);
        }
        resp->r = 0.0;
        resp->i = 0.0;

        for (i=0;i!=Coarse;i++)
        {
                resp1.r = 0.0;
                resp1.i = 0.0;

                for (j=0;j!=Fine;j++)
                {
                        resp1.r += weight[i*Fine+j]*e_resp[j].r;
                        resp1.i += weight[i*Fine+j]*e_resp[j].i;

                }
                tx_rx(f,i,&tmp);
                resp2.r = tmp.r*o_resp[i].r - tmp.i*o_resp[i].i;
                resp2.i = tmp.r*o_resp[i].i + tmp.i*o_resp[i].r;
                resp->r += resp2.r*resp1.r - resp2.i*resp1.i;
                resp->i += resp2.r*resp1.i + resp2.i*resp1.r;

        }
}

double ideal(f)
double f;
{
        int i,j;
        complex resp;
        void i_resp();

        i_resp(f, &resp);
        return(sqrt(resp.i*resp.i+resp.r*resp.r));
}

void i_resp(f, resp)
double f;
complex *resp;
{
        void o_del_resp();
        void e_del_resp();
        void tx_rx();
        void filter_init();

        complex o_resp[10], e_resp[10];
        int i, j;
        complex tmp, resp1, resp2;


        for (i=0;i!=Coarse;i++)
        {
                o_del_resp(f,i, &o_resp[i]);
        }
        for (i=0;i!=Fine;i++)
```

```
                {
                                e_del_resp(f,i,&e_resp[i]);
                }

                resp->r = 0.0;
                resp->i = 0.0;

                for (i=0;i!=Coarse;i++)
                {
                                resp1.r = 0.0;
                                resp1.i = 0.0;

                                for (j=0;j!=Fine;j++)
                                {
                                                resp1.r += weight[i*Fine+j]*e_resp[j].r;
                                                resp1.i += weight[i*Fine+j]*e_resp[j].i;

                                }
                                tmp.r = 1.0;
                                tmp.i = 0.0;

                                resp2.r = tmp.r*o_resp[i].r - tmp.i*o_resp[i].i;
                                resp2.i = tmp.r*o_resp[i].i + tmp.i*o_resp[i].r;
                                resp->r += resp2.r*resp1.r - resp2.i*resp1.i;
                                resp->i += resp2.r*resp1.i + resp2.i*resp1.r;

                }
}

void filter_init(lower, upper, n, m)
double lower, upper;
int n, m;

{
                int i, j;
                void bandpass();
                void new_filter();

printf("filter_init  %e %e %i %i \n", lower, upper, n, m);

                DT = 1.0;
                Coarse = n;
                Fine = m;
                bandpass(lower, upper, Coarse*Fine, weight);

                for (i=0;i!=n;i++)
                                o_delay[i] = (double)(i*m);
                for (j=0;j!=m;j++)
                                e_delay[j] = (double)(j);

                new_filter();
                f_init = 1;
 }

 void e_del_resp(f, i, resp)
 double f;
 int i;
 complex *resp;

 {
                double r;
                r = -e_delay[i]*DT*2.0*pi*f;

                resp->r = cos(r);
                resp->i = sin(r);
 }

 void o_del_resp(f, i, resp)
 double f;
 int i;
 complex *resp;

 {
                double r;
                r = -o_delay[i]*DT*2.0*pi*f;

                resp->r = cos(r);
                resp->i = sin(r);
 }


 static double filter_f[Max_Coarse][ Max_Order] = {1.0};
 static int tx_rx_init = 0;
 static double freq_span = 1.0;
 static double lower_freq = 1.0;
 static int f_order = 1;


 void new_filter()
 {
                int i, j;
```

```
        double drand48();
        void init_tx_rx();

        if (tx_rx_init == 0)
        {
                printf("Auto_tx_rx_init:  span=1.0, lower frequency=1.0, order=1\n");
                init_tx_rx(1.0, 1.0, 1);
        }
        for (j=0;j!=f_order;j++)
        {
                for (i=0;i!=Coarse;i++)
                {
                        filter_f[i][j] = drand48()*freq_span + lower_freq;
                }
        }
}

void init_tx_rx(span, lower, order)
double span, lower;
int order;
{
        freq_span = span;
        lower_freq = lower;
        f_order = order;
        tx_rx_init = 1;
}

void tx_rx(f, i, resp)
double f;
int i;
complex *resp;
{
        int j;
        complex tmp;

        j = 0;
        f = f/filter_f[i][j];
        resp->r = 1.0/(1.0 + f*f);
        resp->i = - f*resp->r;

        while (j!=f_order)
        {
                f = (f/filter_f[i][j]);
                resp->r = 1.0/(1.0 + f*f);
                resp->i = - f * resp->r;
                j++;
        }

}
void init_stat(mean, var, i)
double mean[], var[];
int i;
{
        int j;

        for (j=0;j!=i;j++)
        {
                mean[j]=var[j] = 0.0;
        }
}

void update_stat(resp, mean, var, i)
double resp;
double mean[], var[];
int i;

{
        mean[i] += resp;
        var[i] += resp*resp;
}

void get_stat(mean, var, runs, count)
double mean[], var[];
int count, runs;
{
        int i;
        double num_runs;

        num_runs = runs;

        for (i=0 ;i!=count; i++)
        {
                mean[i] = mean[i] / num_runs;
                var[i] = var[i] / num_runs;
                var[i] = sqrt(fabs(var[i] - mean[i]*mean[i]));
        }
}
```

Listing C.3 model.h

```
#define Num_Samples 100
#define Num_Runs 100
```

```
#define Max_Coarse 10
#define Max_Fine 10
#define Max_Order 10

void bandpass();
void get_stat();
void update_stat();
void init_stat();
void f_resp();
void tx_rx();
void e_del_resp();
void new_filter();
void o_del_resp();
void filter_init();
double ideal();
void init_tx_rx();
```

Listing C.4 Complex.c

```
#include <math.h>
#include "complex.h"
void Cadd(a, b, c)
complex *a, *b, *c;
{
        c->r = a->r+b->r;
        c->i = a->i+b->i;
}
void Csub(a,b,c)
complex *a, *b, *c;
{
        c->r = a->r-b->r;
        c->i = a->i-b->i;
}
void Cdiv(a,b,c)
complex *a, *b, *c;
{
        double r, den;
        if (fabs(b->r) >=fabs(b->i))
        {
                r = b->i/b->r;
                den = b->r + r*b->i;
                c->r = (a->r+r*a->i)/den;
                c->i = (a->i - r*a->r)/den;
        } else {
                r = b->r/b->i;
                den = b->i + r*b->r;
                c->r = (a->r*r + a->r)/den;
                c->i = (a->i*r - a->r)/den;
        }
}
void Cmul(a, b, c)
complex *a, *b, *c;
{
        c->r = a->r*b->r - a->i*b->i;
        c->i = a->r*b->i + a->i*b->r;
}
void Complex(re, im, c)
double re, im;complex *c;
{
        c->r = re;
        c->i = im;
}
double Cabs(c)
complex *c;
{
        return(sqrt(c->i*c->i+c->r*c->r));
}
void Conjg(c, z)
complex *c, *z;
{
        z->r = c->r;
        z->i = -c->i;
}
void Csqrt(z, c)
complex *c, *z;
{
        double x,y,w,r;
        if ((z->r==0.0) && (z->i == 0.0))
        {
                c->r = c->i = 0.0;
                return;
        } else {
                x = fabs(z->r);
                y = fabs(z->i);
                if (x >= y)
                {
                        r = y/x;
                        w = sqrt(x)*sqrt(0.5*(1.0+sqrt(1.0+r*r)));
                } else {
                        r = x/y;
                        w = sqrt(y)*sqrt(0.5*(r+sqrt(1.0+r*r)));
                }
                if (z->r >=0.0)
```

```
                        {
                                        c->r = w;
                                        c->i = z->i/(2.0*w);
                        } else {
                                        c->i = (z->i >= 0.0) ? w:-w;
                                        c->r = z->i / (2.0*c->i);
                        }
            }
}
void RCmul(x, z, c)
double x;complex *c, *z;
{
            c->r = x*z->r;
            c->i = x*z->i;
}
void RCdiv(x, z, c)
double x;
complex *c, *z;
{
            c->r = z->r / x;
            c->i = z->i / x;
}
void Cexp(z, c)
complex *c, *z;
{
            double r;
            r = exp(z->r);
            c->i = r*sin(z->i);
            c->r = r*cos(z->i);
}
void Cmove(z, c)
complex *z, *c;
{
            c->r = z->r;
            c->i = z->i;
}
```

Listing C.5 Complex.c

```
typedef struct COMPLEX {double r, i;} complex;

extern void Cadd();
extern void Csub();
extern void Cdiv();
extern void Cmul();
extern void Complex();
extern double Cabs();
extern void Conjg();
extern void Csqrt();
extern void RCmul();
extern void RCdiv();
extern void Cexp();
extern void Cmove();
```

Listing C.6 An example of input data file

```
0.5         <=frequency span
1           <=lower frequency limit
5           <=order of the filter
0.2         <=lower bandpass frequency
0.4         <=upper bandpass frequency
5           <=number of coarse delay increments
4           <=number of fine delay increments
789098      <=seed for the random generator
```

The second program is used to model the effects of the delay time variation on the FIR filter response. In this version, the variation parameters are a part of the programming code. The variable for determining the time fluctuation is 'delta' in model.c module. After every modification, the program is required to be re-compiled.

This program also consists of 5 files: model.c, model.h, main.c, complex.c, and complex.h. Only two files, model.c and main.c, are different from the first program. The following is the listings of the two different files:

Listing C.5 Main.c (for the delay time simulation)

```
#include <stdio.h>
#include <math.h>
#include "complex.h"
#include "model.h"

#define Span 1.0
#define Lower_freq 2.0
#define Order 1
#define Lower_corner 0.2
#define Upper_corner 0.4
#define Coarse 5
#define Fine 5

double pi;

main()
{
        complex resp;
        double mean[Num_Samples];
        double var[Num_Samples];
        int i, j, n, m;
        double f, df, tmp;
        double tmp1,drand48();
        pi = 4.0 * atan(1.0);
        init_tx_rx(Span, Lower_freq, Order);
        filter_init(Lower_corner, Upper_corner, Coarse, Fine);
        printf("rx_tx spec:  span=%e\n", Span);
        printf("            lower_freq=%e\n", Lower_freq);
        printf("            order=%i\n",Order);
        printf("filter spec: lower corner=%e\n", Lower_corner);
        printf("            upper corner=%e\n", Upper_corner);
        printf("            fine increments=%i\n", Fine);
        printf("            coarse increments=%i\n", Coarse);
        init_stat(mean, var, Num_Samples);
        df = 1.0/2.0/Num_Samples;
        for (i=0; i!=Num_Runs; i++) {
                new_filter();
                f = 0.0;
                for (j=0; j!=Num_Samples; j++) {
                        f_resp(f, &resp);
                        tmp = sqrt(resp.r*resp.r + resp.i*resp.i);
                        update_stat(tmp, mean, var, j);
                        f += df;
                };
        };
        get_stat(mean, var, Num_Runs, Num_Samples);
        f = 0.0;
        printf("freq\t\t\t\tupper\t\t\t\tlower\t\t\tideal\n");
        for (i=0;i!=Num_Samples; i++) {
                printf("%e\t",f);
                printf("%e\t%e\t%e\n", mean[i]+var[i], mean[i]-var[i], ideal(f));
                f += df;
        };
}
```

Listing C.8 Model.c (for the delay time simulation)

```
#include <math.h>
#include <stdio.h>
#include "complex.h"
#include "model.h"
extern double pi;
static double delta=0.01;  /* 10% change in delay time. */
static double weight[Max_Coarse * Max_Fine] = {0.0};
static double e_delay [Max_Fine] = {0.0};
static double o_delay [Max_Coarse] = {0.0};
static int f_init=0;
static double DT;
static int Coarse = 10;
static int Fine = 10;
void bandpass (lower, upper, taps, weights)
double lower;
double upper;
int taps;
double weights[];
{
        int i;
        for (i=0; i!=taps/2 + 1; i++) {
                if (i == 0) {
                        weights[taps/2] = (upper - lower) / 0.5;
                } else {
                        weights[taps/2 - i] = weights[taps/2 + i] =
                        1.0/pi/i*(sin(2.0*i*upper*pi) - sin(2.0*i*lower*pi));
                }
        }
        for (i=0;i!=taps;i++)
                        printf("%i %e\n", i, weights[i]);

}
void f_resp(f, resp)
double f;
```

```
complex *resp;
{
        void o_del_resp();
        void e_del_resp();
        void tx_rx();
        void filter_init();
        complex resp1, resp2, tmp;


        complex o_resp[10], e_resp[10];
        int i, j;
        if (f_init == 0) {
                printf("auto_init()\n");
                filter_init(0.1, 0.25, Max_Fine, Max_Coarse);
                }
        for (i=0;i!=Coarse;i++) {
                o_del_resp(f,i, &o_resp[i]);
        }
        for (i=0;i!=Fine;i++) {
                e_del_resp(f,i,&e_resp[i]);
        }
        resp->r = 0.0;
        resp->i = 0.0;
        for (i=0;i!=Coarse;i++) {
                resp1.r = 0.0;
                resp1.i = 0.0;
                for (j=0;j!=Fine;j++) {
                        resp1.r += weight[i*Fine+j]*e_resp[j].r;
                        resp1.i += weight[i*Fine+j]*e_resp[j].i;
                }
                tx_rx(f,i,&tmp);
                resp2.r = tmp.r*o_resp[i].r - tmp.i*o_resp[i].i;
                resp2.i = tmp.r*o_resp[i].i + tmp.i*o_resp[i].r;
                resp->r += resp2.r*resp1.r - resp2.i*resp1.i;
                resp->i += resp2.r*resp1.i + resp2.i*resp1.r;
        }
}

double ideal(f)
double f;
{
        int i,j;
        complex resp;
        void i_resp();
        double tmp;
/* adhoc solution for the random delta time problem */
        tmp = delta;
        delta = 0.0;
        i_resp(f, &resp);
/* adhoc solution for the random delta time problem */
        delta = tmp;
        return(sqrt(resp.i*resp.i+resp.r*resp.r));
}
void i_resp(f, resp)
double f;
complex *resp;
{
        void o_del_resp();
        void e_del_resp();
        void tx_rx();
        void filter_init();
        complex o_resp[10], e_resp[10];
        int i, j;
        complex tmp, resp1, resp2;
        for (i=0;i!=Coarse;i++) {
                o_del_resp(f,i, &o_resp[i]);
        }
        for (i=0;i!=Fine;i++) {
                e_del_resp(f,i,&e_resp[i]);
        }
        resp->r = 0.0;
        resp->i = 0.0;
        for (i=0;i!=Coarse;i++) {
                resp1.r = 0.0;
                resp1.i = 0.0;
                for (j=0;j!=Fine;j++) {
                        resp1.r += weight[i*Fine+j]*e_resp[j].r;
                        resp1.i += weight[i*Fine+j]*e_resp[j].i;
                }
                tmp.r = 1.0;
                tmp.i = 0.0;
                resp2.r = tmp.r*o_resp[i].r - tmp.i*o_resp[i].i;
                resp2.i = tmp.r*o_resp[i].i + tmp.i*o_resp[i].r;
                resp->r += resp2.r*resp1.r - resp2.i*resp1.i;
                resp->i += resp2.r*resp1.i + resp2.i*resp1.r;
        }
}
void filter_init(lower, upper, n, m)
double lower, upper;
int n, m;
{
        int i, j;
        void bandpass();
        void new_filter();
        DT = 1.0;
        Coarse = n;
        Fine = m;
        bandpass(lower, upper, Coarse*Fine, weight);
        for (i=0;i!=n;i++)
                o_delay[i] = (double)(i*m);
        for (j=0;j!=m;j++)
                e_delay[j] = (double)(j);
        new_filter();
        f_init = 1;
}
void e_del_resp(f, i, resp)
double f;
int i;
complex *resp;
{
        double r;
        double drand48();
        r = -(1.0+delta*drand48())*e_delay[i]*DT*2.0*pi*f;
        resp->r = cos(r);
        resp->i = sin(r);
}
void o_del_resp(f, i, resp)
double f;
int i;
complex *resp;
{
        double r;
        double drand48();
        r = -(1.0+delta*drand48())*o_delay[i]*DT*2.0*pi*f;
        resp->r = cos(r);
        resp->i = sin(r);
}
static double filter_f[Max_Coarse][ Max_Order] = {1.0};
static int tx_rx_init = {0};
static double freq_span = 1.0;
static double lower_freq = 1.0;
static int f_order = 1;
void new_filter()
{
        int i, j;
        double drand48();
        void init_tx_rx();
        if (tx_rx_init == 0) {
                printf("Auto_tx_rx_init:  span=1.0, lower frequency=1.0, order=1\n");
                init_tx_rx(1.0, 1.0, 1);
        }
        for (j=0;j!=f_order;j++) {
                for (i=0;i!=Coarse;i++) {
                        /* change this to fix frequency */
                        filter_f[i][j] = freq_span/2.0 + lower_freq;
                }
        }
}
void init_tx_rx(span, lower, order)
double span, lower;
int order;
{
        freq_span = span;
        lower_freq = lower;
        f_order = order;
        tx_rx_init = 1;
}
void tx_rx(f, i, resp)
double f;
int i;
complex *resp;
{
        int j;
        complex tmp;
        for (j=0;j!=f_order; j++) {
                f = (f/filter_f[i][j]);
                resp->r = 1.0/(1.0 + f*f);
                resp->i = - f*resp->r;
        }

}
void init_stat(mean, var, i)
double mean[], var[];
int i;
{
        int j;
        for (j=0;j!=i;j++) {
                mean[j]=var[j] = 0.0;
        }
}
void update_stat(resp, mean, var, i)
double resp;
double mean[], var[];
int i;
```

```
 {
                mean[i] += resp;
                var[i] += resp*resp;
 }
void get_stat(mean, var, runs, count)
double mean[], var[];
int count, runs;
{
                int i;
                double num_runs;
                num_runs = runs;
                for (i=0 ;i!=count; i++) {
                                mean[i] = mean[i] / num_runs,
                                var[i] = var[i] / num_runs;
                                var[i] = sqrt(fabs(var[i] - mean[i]*mean[i]));
                }
}
```

Appendix D The Detail Transmitter Circuit Diagram

This appendix contains the detail circuit diagram and the printed circuit board design of the transmitter card.

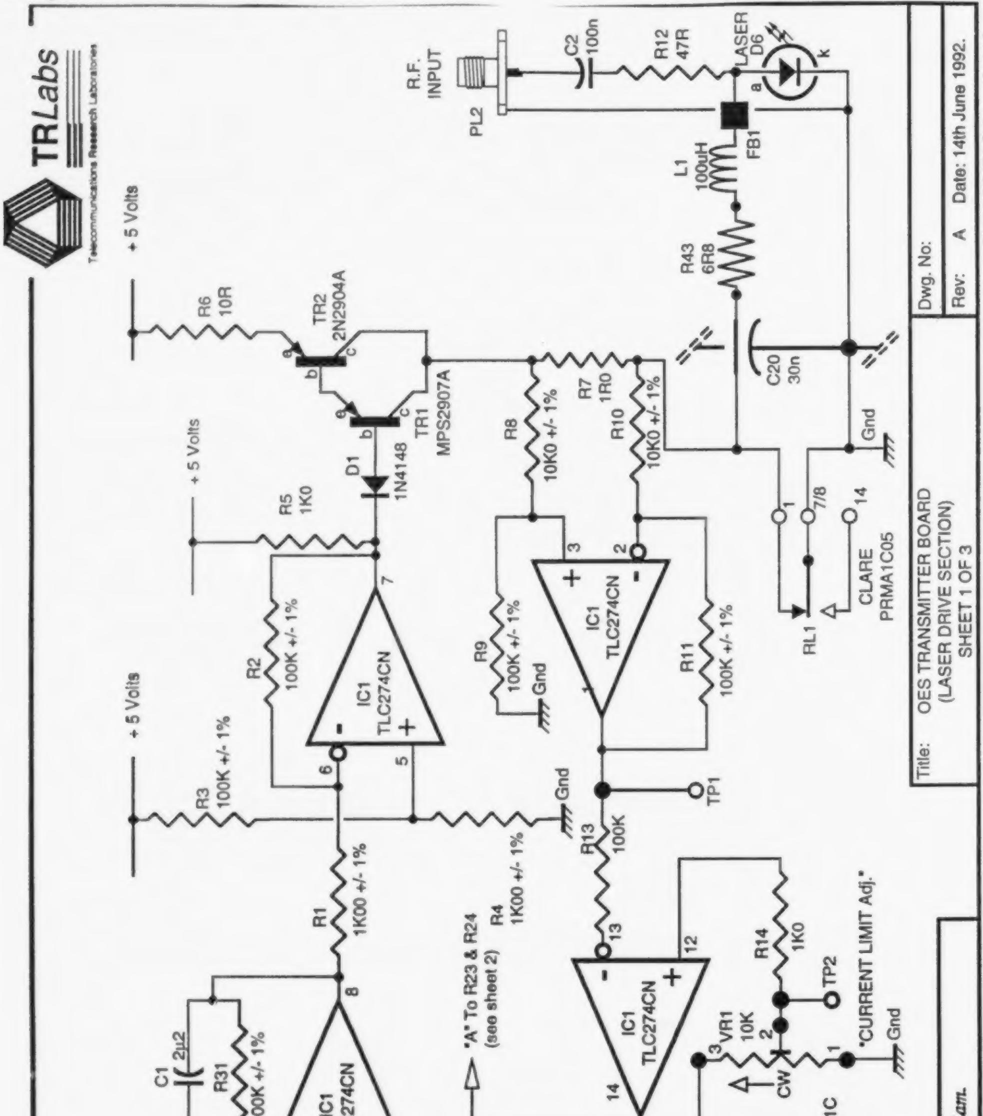

TRLabs
Telecommunications Research Laboratories
+ 5 Volts
R6 10R
TR2 2N2904A
TR1 MPS2907A
D1 1N4148
R5 1K0
R2 100K +/- 1%
IC1 TLC274CN
R3 100K +/- 1%
R1 1K00 +/- 1%
R4 1K00 +/- 1%
C1 2µ2
R31 100K +/- 1%
C11 2µ2
"C" From R30 (see sheet 3)
"B" From R26 (see sheet 2)
"A" To R23 & R24 (see sheet 2)
Gnd
R8 10K0 +/- 1%
R7 1R0
R10 10K0 +/- 1%
R9 100K +/- 1%
R11 100K +/- 1%
R13 100K
TP1
TP2
R14 1K0
VR1 10K
CW
"CURRENT LIMIT Adj."
R15 1K2
IC2 TL431C
ref
C3 10µ
R.F. INPUT
PL2
C2 100n
R12 47R
LASER D6
FB1
L1 100uH
R43 6R8
C20 30n
RL1
CLARE PRMA1C05
1
7/8
14
Title: OES TRANSMITTER BOARD (LASER DRIVE SECTION) SHEET 1 OF 3
Dwg. No:
Rev: A Date: 14th June 1992.
File: OES TX Schematic-01A
Drawn By: Dobby Lam.

Figure D.1 Transmitter circuit diagram (1 out of 5)

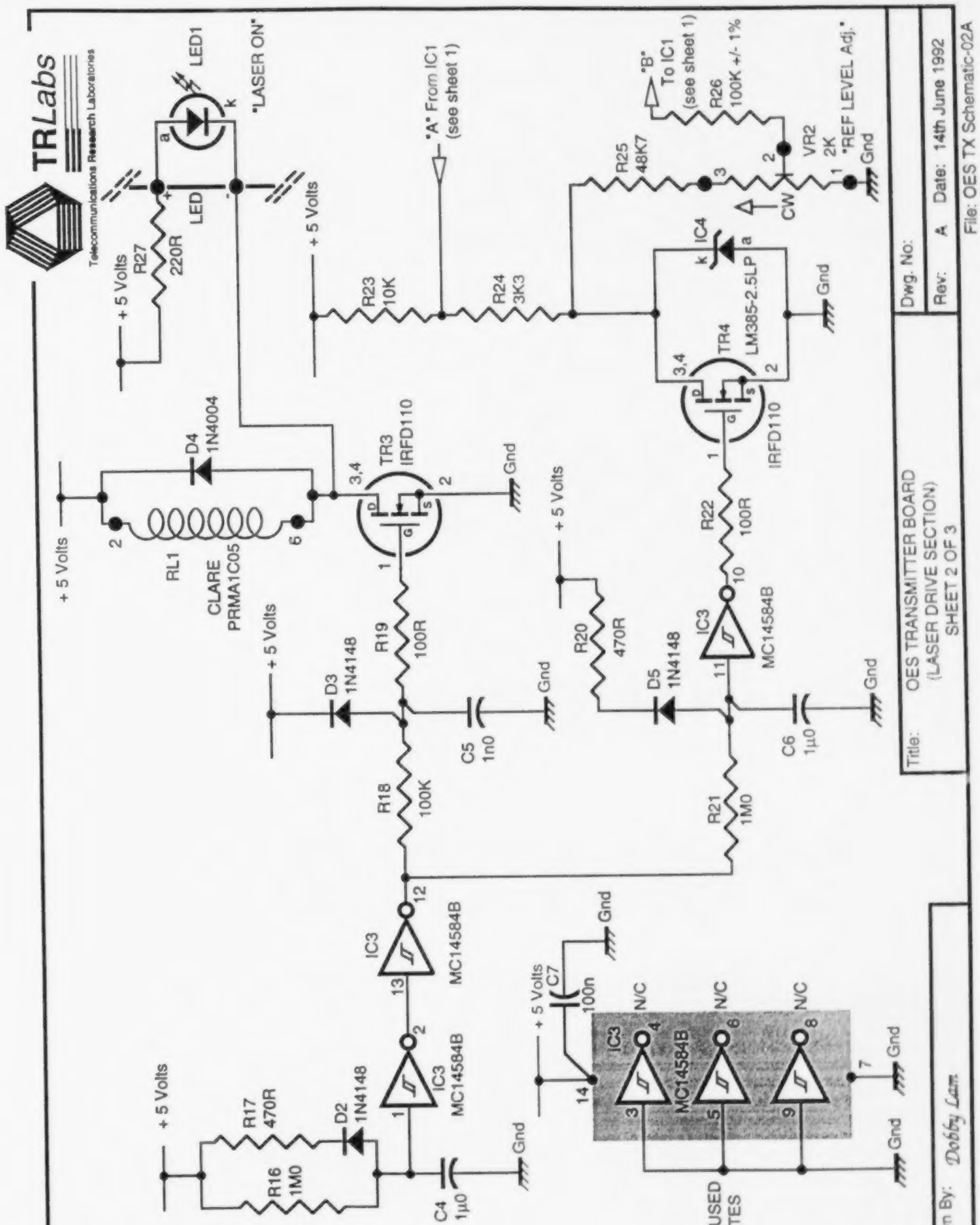
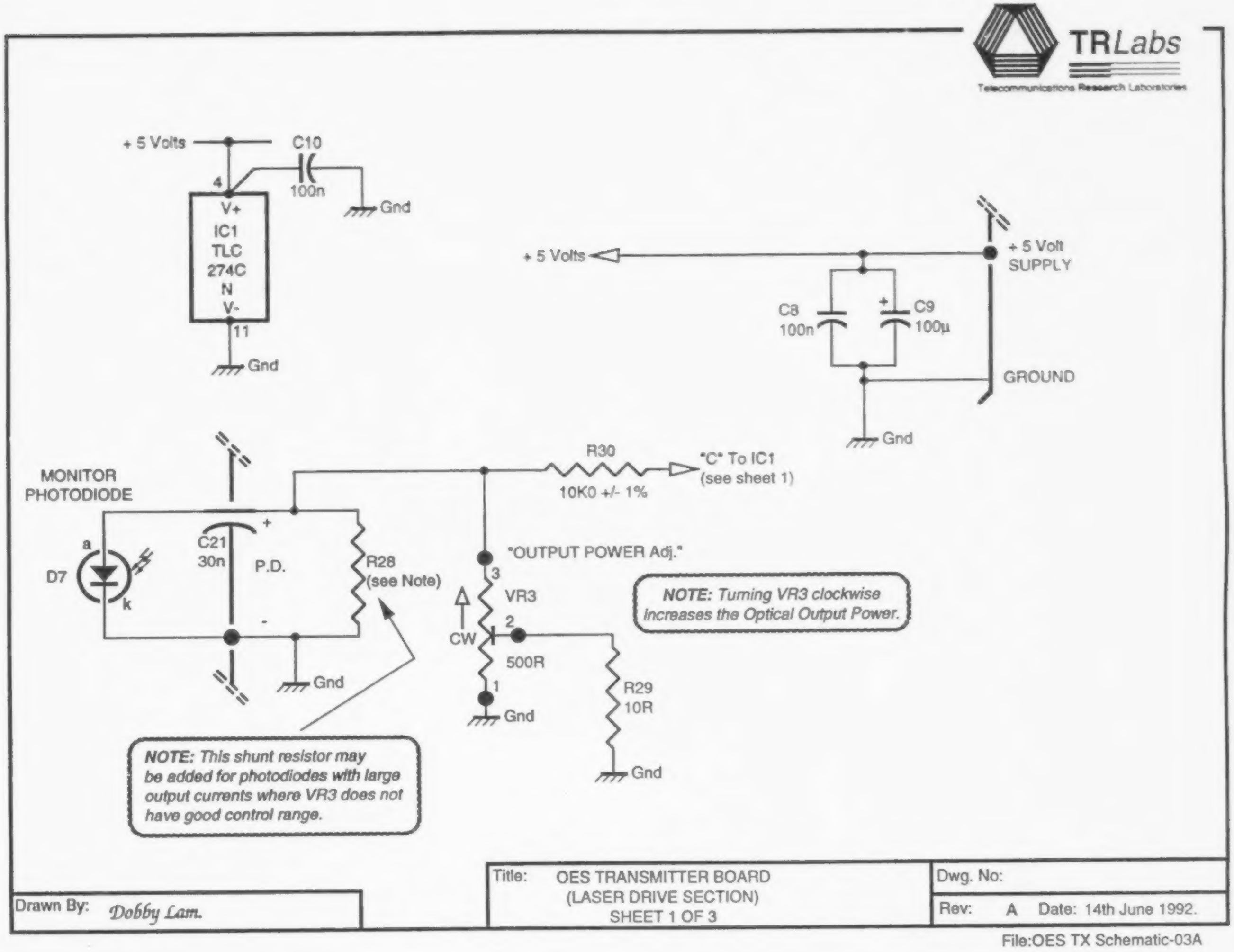

TRLabs
Telecommunications Research Laboratories
+ 5 Volts
R27
220R
LED
+
-
a
k
LED1
"LASER ON"
+ 5 Volts
R23
10K
"A" From IC1
(see sheet 1)
R24
3K3
R25
48K7
"B"
To IC1
(see sheet 1)
R26
100K +/- 1%
3
2
1
VR2
2K
"REF LEVEL Adj."
CW
Gnd
IC4
k
a
LM385-2.5LP
Gnd
TR4
3,4
2
1
IRFD110
d
g
s
R22
100R
10
IC3
MC14584B
11
D5
1N4148
R20
470R
+ 5 Volts
C6
1µ0
Gnd
R21
1M0
+ 5 Volts
D4
1N4004
RL1
CLARE
PRMA1C05
2
6
TR3
IRFD110
3,4
2
1
Gnd
R19
100R
D3
1N4148
+ 5 Volts
C5
1n0
Gnd
R18
100K
12
IC3
MC14584B
13
2
IC3
MC14584B
1
+ 5 Volts
R17
470R
D2
1N4148
R16
1M0
C4
1µ0
Gnd
+ 5 Volts
C7
100n
Gnd
14
IC3
MC14584B
N/C
4
N/C
6
N/C
8
3
5
9
7
Gnd
Gnd
UNUSED
GATES
Title:
OES TRANSMITTER BOARD
(LASER DRIVE SECTION)
SHEET 2 OF 3
Dwg. No:
Rev:
A
Date: 14th June 1992
File: OES TX Schematic-02A
Drawn By:
Dobby Lam

Figure D.1 Transmitter circuit diagram (2 out of 5)


TRLabs
Telecommunications Research Laboratories
+ 5 Volts
C10
100n
Gnd
4
V+
IC1
TLC
274C
N
V-
11
Gnd
+ 5 Volts
+ 5 Volt
SUPPLY
C8
100n
C9
100µ
+
GROUND
Gnd
MONITOR
PHOTODIODE
a
D7
k
C21
30n
+
P.D.
-
R28
(see Note)
Gnd
R30
10K0 +/- 1%
"C" To IC1
(see sheet 1)
"OUTPUT POWER Adj."
3
VR3
2
CW
500R
1
Gnd
R29
10R
Gnd
Title:
OES TRANSMITTER BOARD
(LASER DRIVE SECTION)
SHEET 1 OF 3
Dwg. No:
Rev:
A
Date: 14th June 1992.
Drawn By:
Dobby Lam.
File:OES TX Schematic-03A

NOTE: *This shunt resistor may be added for photodiodes with large output currents where VR3 does not have good control range.*

NOTE: *Turning VR3 clockwise increases the Optical Output Power.*

Figure D.1 Transmitter circuit diagram (3 out of 5)

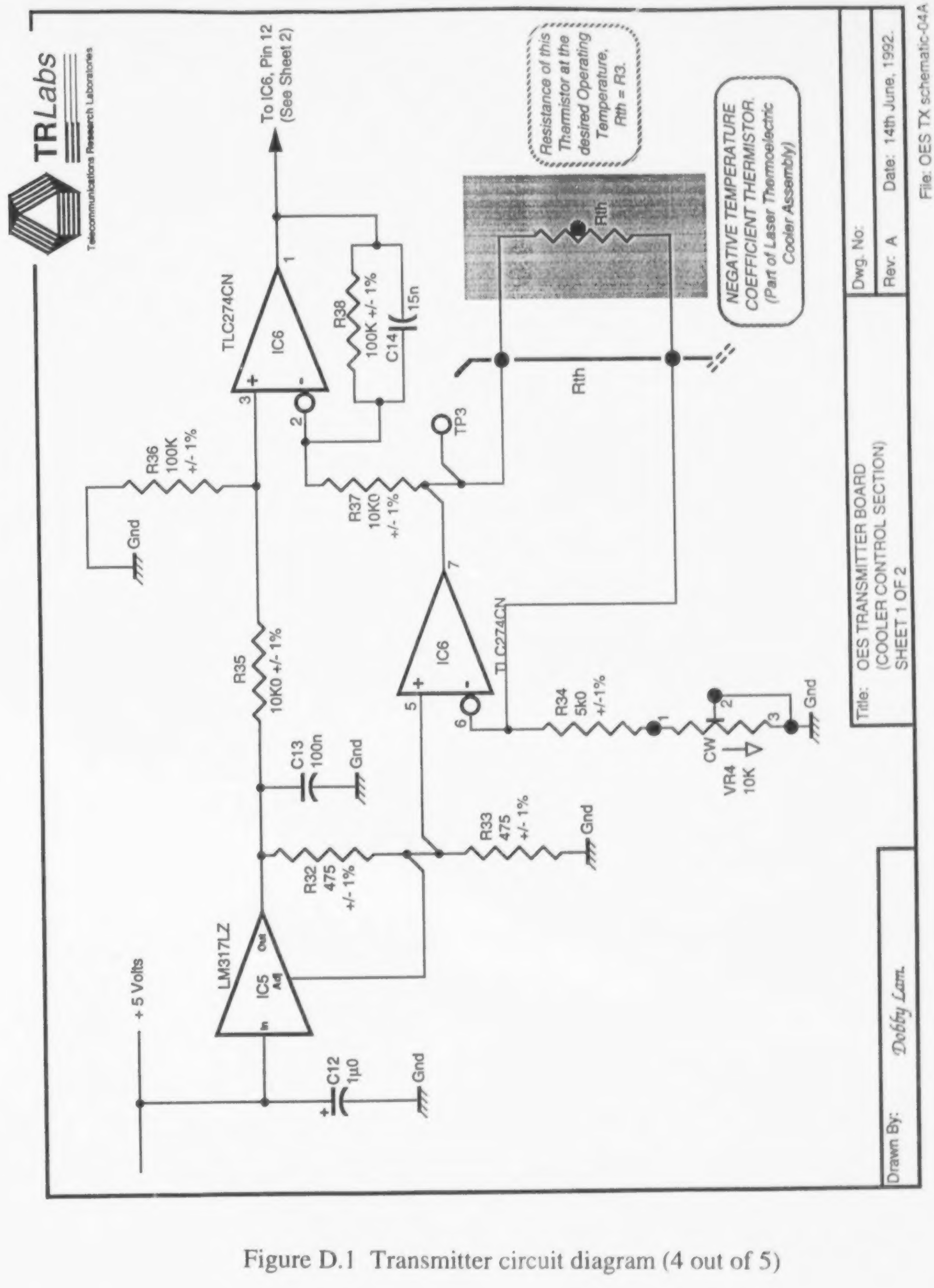

TRLabs
Telecommunications Research Laboratories
To IC6, Pin 12
(See Sheet 2)
TLC274CN
IC6
1
2
3
R38
100K +/- 1%
C14
15n
Rth
Resistance of this Thermistor at the desired Operating Temperature, Rth = R3.
NEGATIVE TEMPERATURE COEFFICIENT THERMISTOR.
(Part of Laser Thermoelectric Cooler Assembly)
TP3
R36
100K
+/- 1%
Gnd
R37
10K0
+/- 1%
7
TLC274CN
IC6
5
6
R35
10K0 +/- 1%
C13
100n
Gnd
R34
5K0
+/-1%
VR4
10K
CW
Gnd
R33
475
+/- 1%
Gnd
R32
475
+/- 1%
LM317LZ
IC5
In
Out
Adj
+ 5 Volts
C12
1µ0
Gnd
Title: OES TRANSMITTER BOARD
(COOLER CONTROL SECTION)
SHEET 1 OF 2
Dwg. No:
Rev: A
Date: 14th June, 1992.
File: OES TX schematic-04A
Drawn By: Dobby Lam.

Figure D.1 Transmitter circuit diagram (4 out of 5)

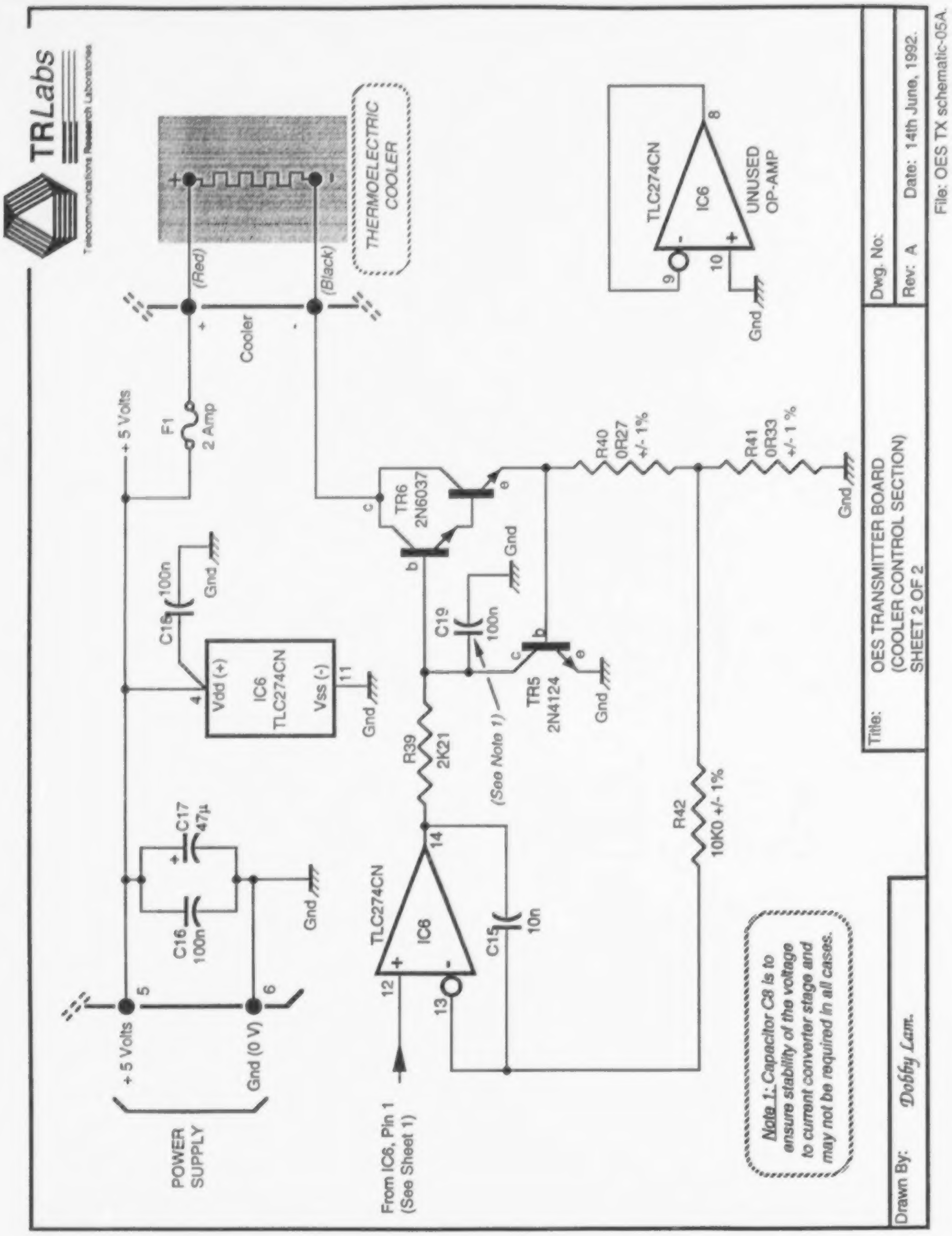

TRLabs
Telecommunications Research Laboratories
THERMOELECTRIC COOLER
(Red)
(Black)
Cooler
+ 5 Volts
F1
2 Amp
TR6
2N6037
c
b
e
R40
0R27
+/- 1%
R41
0R33
+/- 1 %
Gnd
C18
100n
Vdd (+)
IC6
TLC274CN
Vss (-)
4
11
C19
100n
TR5
2N4124
(See Note 1)
R39
2K21
R42
10K0 +/- 1%
C17
47µ
C16
100n
C15
10n
14
12
13
5
6
POWER SUPPLY
+ 5 Volts
Gnd (0 V)
From IC6, Pin 1
(See Sheet 1)
UNUSED
OP-AMP
9
10
8
Note 1: Capacitor C8 is to ensure stability of the voltage to current converter stage and may not be required in all cases.
Title: OES TRANSMITTER BOARD (COOLER CONTROL SECTION) SHEET 2 OF 2
Dwg. No:
Rev: A
Date: 14th June, 1992.
File: OES TX schematic-05A.
Drawn By: Dobby Lam.

Figure D.1 Transmitter circuit diagram (5 out of 5)

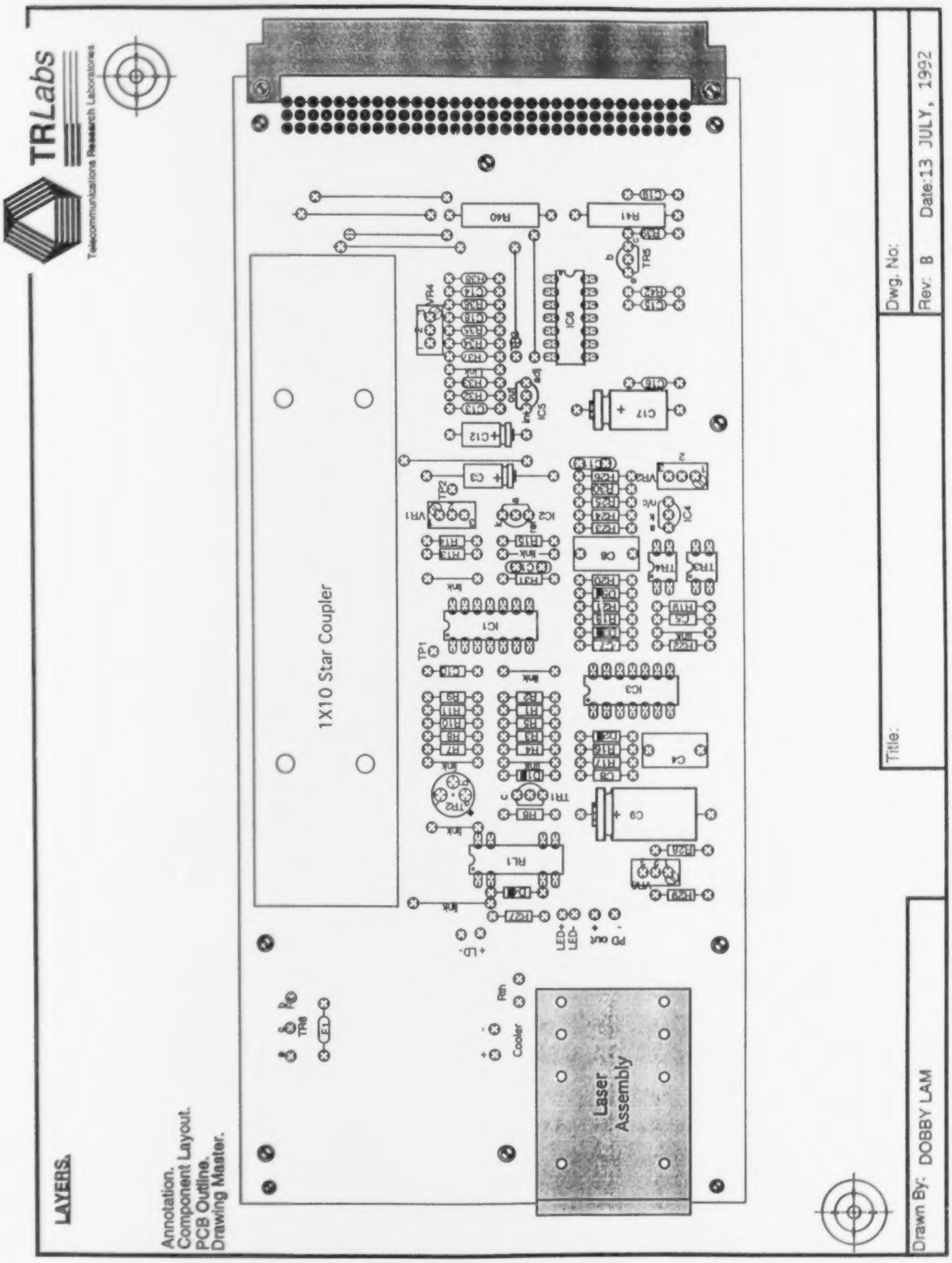

TRLabs
Telecommunications Research Laboratories
LAYERS.
Annotation.
Component Layout.
PCB Outline.
Drawing Master.
1X10 Star Coupler
Laser Assembly
Cooler
Dwg. No:
Rev: B
Date:13 JULY, 1992
Title:
Drawn By: DOBBY LAM

Figure D.2 The layout digram of the transmitter card

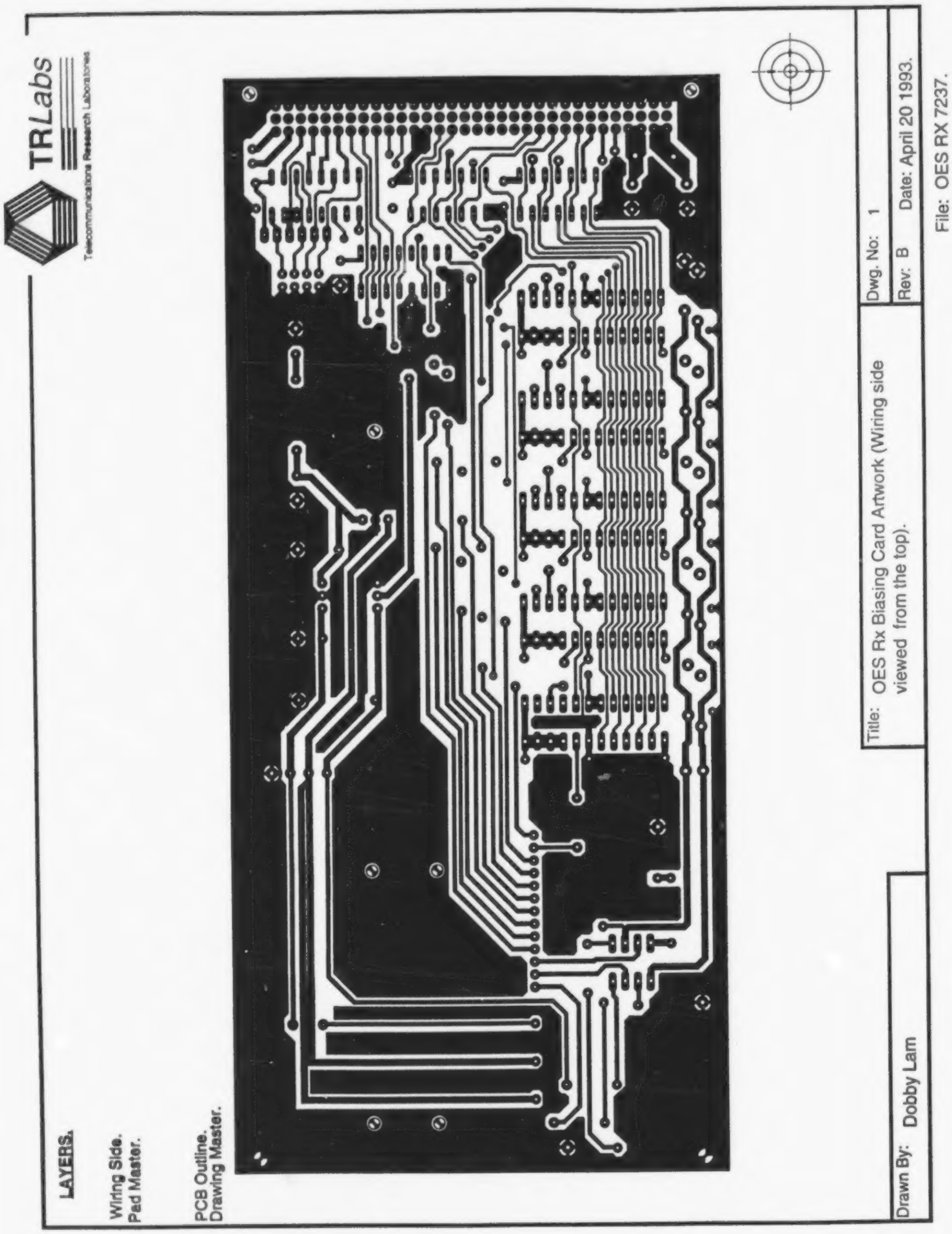

TRLabs
Telecommunications Research Laboratories
LAYERS.
Wiring Side.
Pad Master.
PCB Outline.
Drawing Master.
Title: OES Rx Biasing Card Artwork (Wiring side viewed from the top).
Dwg. No: 1
Rev: B
Date: April 20 1993.
File: OES RX 7237.
Drawn By: Dobby Lam

Figure D.3 The printed circuit design for the transmitter card

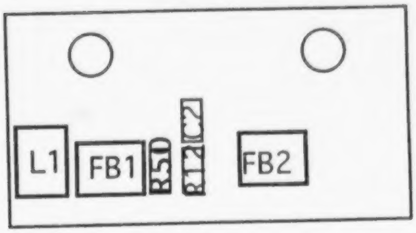

L1
FB1
R51
R12
C2
FB2

Figure D.4 The layout diagram of the Bias/RF insertion unit

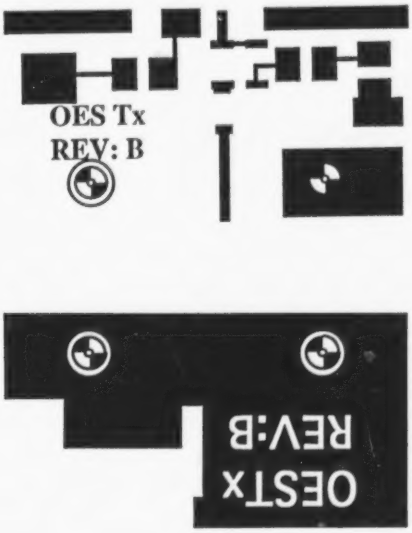

OES Tx
REV: B
OESTx
REV:B

Figure D.5 The printed circuit board design of the Bias/RF insertion unit

APPENDIX E LASER TRANSMITTER OPTICAL MEASUREMENT SETUP AND RESULTS

E.1 Frequency Response Measurement Setup

The setup for characterizing the dynamic response of the laser transmitter is shown in Figure E.1. The center of the setup is a high speed GaAlAs/GaAs PIN photodiode, Ortel model PD050-OM. The photodiode is connected to a dc voltage supply via a Picosecond Pulse model 5575A biasing tee and the output from the diode is fed to one of the ports of a HP-8759A network analyzer with a HP-85064A S-parameter test set. The other port of HP-85046A is connected to the transmitter to modulate the laser diode. The optical output laser is collimated and focused into the PIN diode with a two x40 objectives. The S_{21} response is recorded with a HP-7475A plotter. The test conditions of the ten transmitters are listed in Table E.1; the test results are shown in Figure E.2.

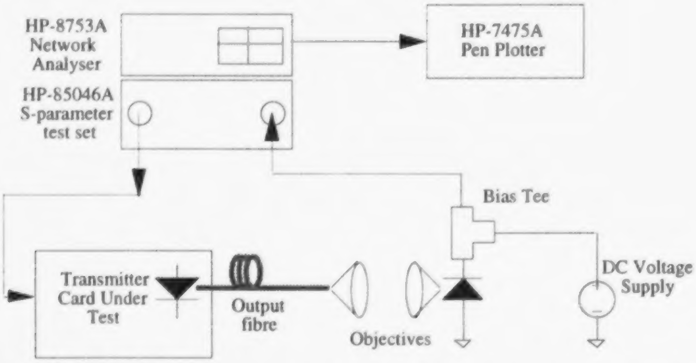

HP-8753A
Network
Analyser
HP-7475A
Pen Plotter
HP-85046A
S-parameter
test set
Bias Tee
Transmitter
Card Under
Test
Output
fibre
Objectives
DC Voltage
Supply

Figure E.1 The frequency response test setup of the transmitter frequency response

Table E.1 The test conditions of the transmitter frequency responses

Transmitter Card Number	3 dB Bandwidth (GHz)	Bias Current (mA)
1	1.34	65.5
2	1.33	62.2
3	1.21	73.3
4	1.65	67.9
5	1.36	66.0
6	1.14	63.5
7	1.26	65.0

8	1.22	67.7
9	1.36	64.0
10	1.31	58.9

E.2 SNR Measurement Setup

The SNR of the laser transmitter, shown in Figure E.1, is similar to the frequency response setup. The network analyzer is replaced with a HP-7000A spectrum analyzer and a HP8753A signal generator.

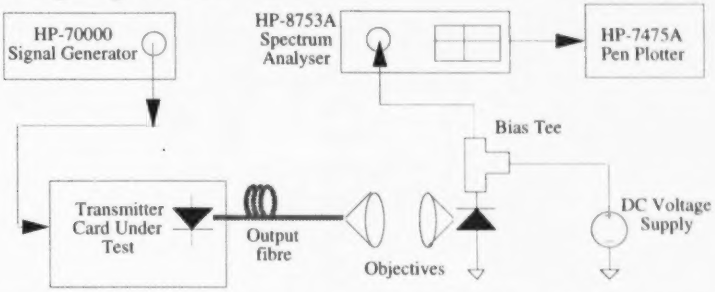

HP-70000
Signal Generator
HP-8753A
Spectrum
Analyser
HP-7475A
Pen Plotter
Bias Tee
Transmitter
Card Under
Test
Output
fibre
Objectives
DC Voltage
Supply

Figure E.2 The noise floor test setup of the transmitter frequency response

Appendix F The Mechanical Drawings and the Assembly Diagram of the Transmitter Card

This appendix contains the mechanical drawings and the assembly diagram of the transmitter card.

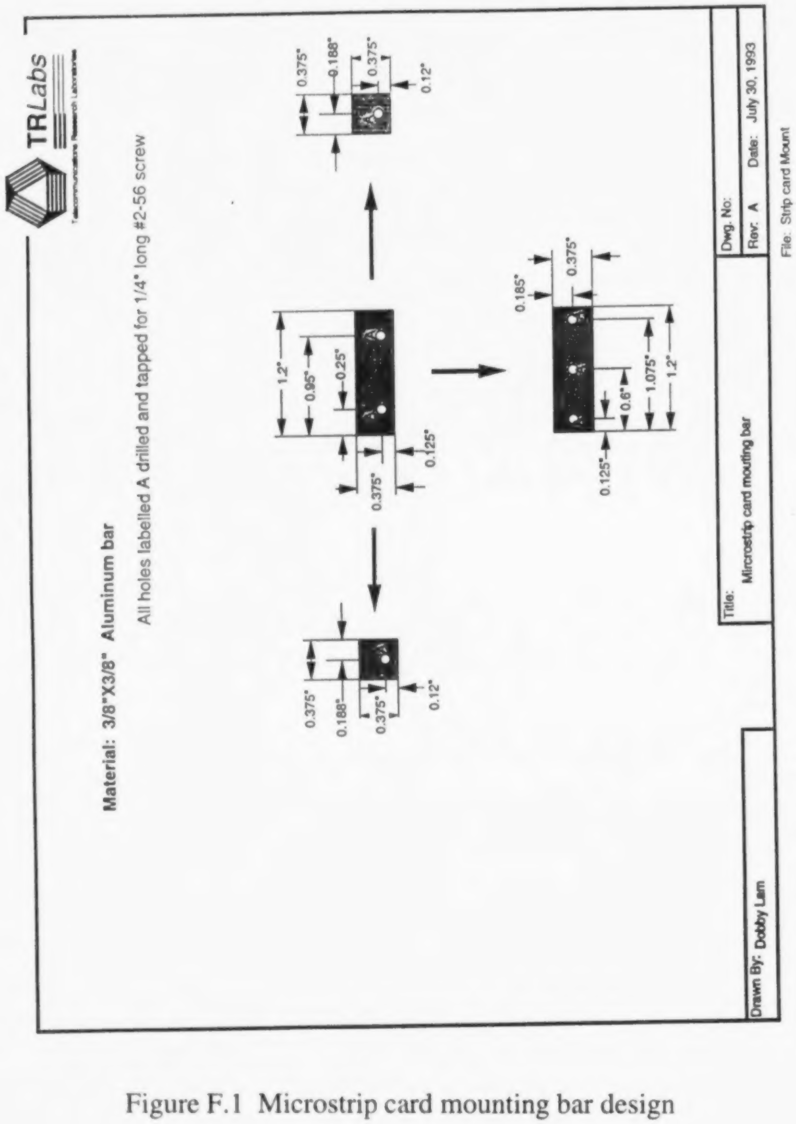

TRLabs
Telecommunications Research Laboratories
Material: 3/8"X3/8" Aluminum bar
All holes labelled A drilled and tapped for 1/4" long #2-56 screw
0.375"
0.188"
0.375"
0.12"
1.2"
0.95"
0.25"
0.125"
0.375"
0.185"
0.375"
0.6"
1.075"
1.2"
0.125"
0.375"
0.188"
0.375"
0.12"
Dwg. No:
Rev: A
Date: July 30, 1993
File: Strip card Mount
Title:
Microstrip card mouting bar
Drawn By: Dobby Lam

Figure F.1 Microstrip card mounting bar design

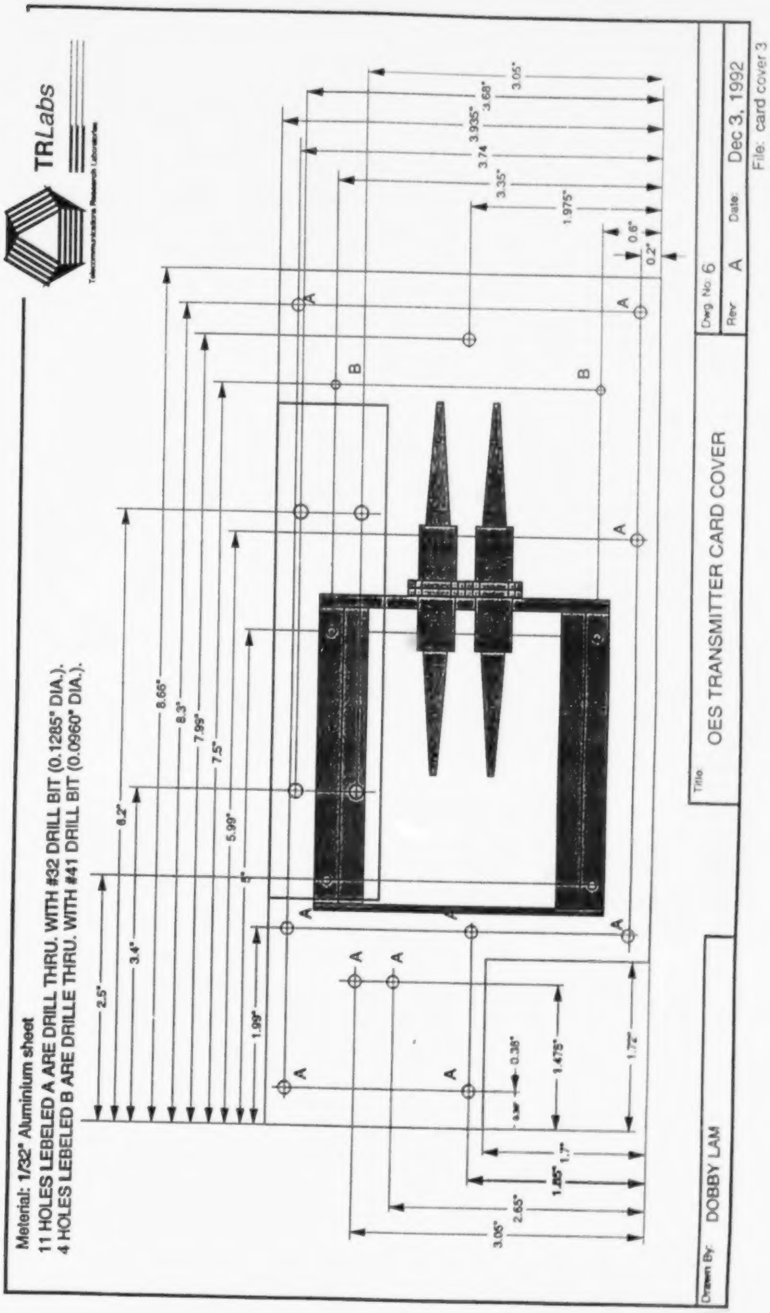

Meterial: 1/32" Aluminium sheet
11 HOLES LEBELED A ARE DRILL THRU. WITH #32 DRILL BIT (0.1285" DIA.).
4 HOLES LEBELED B ARE DRILLE THRU. WITH #41 DRILL BIT (0.0960" DIA.).
TRLabs
Telecommunications Research Laboratories
2.5"
3.4"
8.2"
8.66"
8.3"
7.99"
7.5"
5.99"
5"
1.99"
3.05"
3.68"
3.935"
3.74
3.35"
1.975"
0.6"
0.2"
3.05"
2.65"
1.85"
1.7"
1.72"
1.475"
0.38"
0.38"
A
B
Title
OES TRANSMITTER CARD COVER
Drawn By:
DOBBY LAM
Dwg No: 6
Rev
A
Date:
Dec 3, 1992
File: card cover 3

Figure F.2 Transmitter card cover design

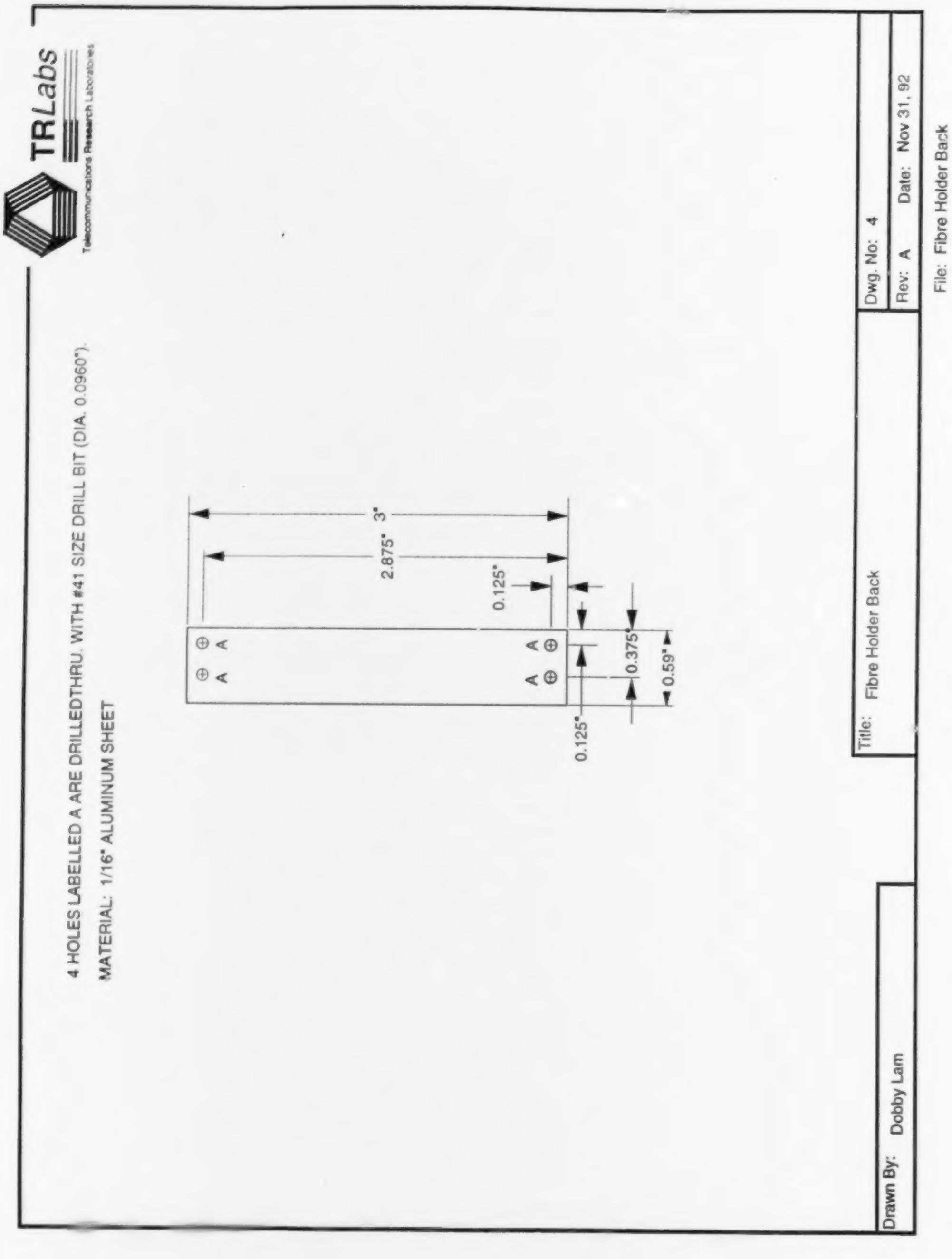

TRLabs
Telecommunications Research Laboratories
4 HOLES LABELLED A ARE DRILLEDTHRU. WITH #41 SIZE DRILL BIT (DIA. 0.0960").
MATERIAL: 1/16" ALUMINUM SHEET
3"
2.875"
0.125"
A
A
A
A
0.375"
0.59"
0.125"
Drawn By: Dobby Lam
Title: Fibre Holder Back
Dwg. No: 4
Rev: A
Date: Nov 31, 92
File: Fibre Holder Back

Figure F.3 Fiber holder back design

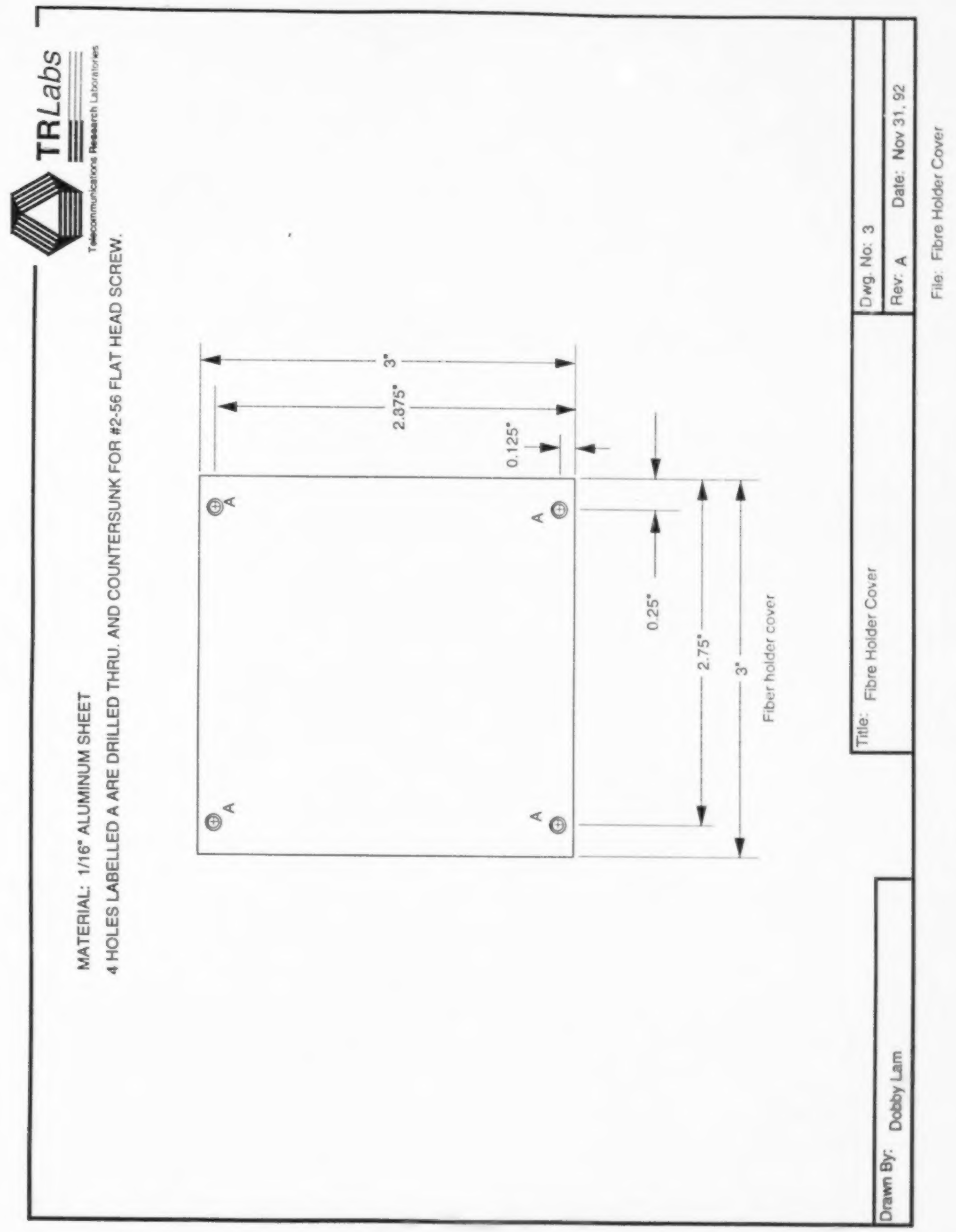

TRLabs
Telecommunications Research Laboratories
MATERIAL: 1/16" ALUMINUM SHEET
4 HOLES LABELLED A ARE DRILLED THRU. AND COUNTERSUNK FOR #2-56 FLAT HEAD SCREW.
3"
2.375"
0.125"
A
A
A
A
0.25"
2.75"
3"
Fiber holder cover
Title: Fibre Holder Cover
Dwg. No: 3
Rev: A
Date: Nov 31, 92
File: Fibre Holder Cover
Drawn By: Dobby Lam

Figure F.4 Fiber holder cover design

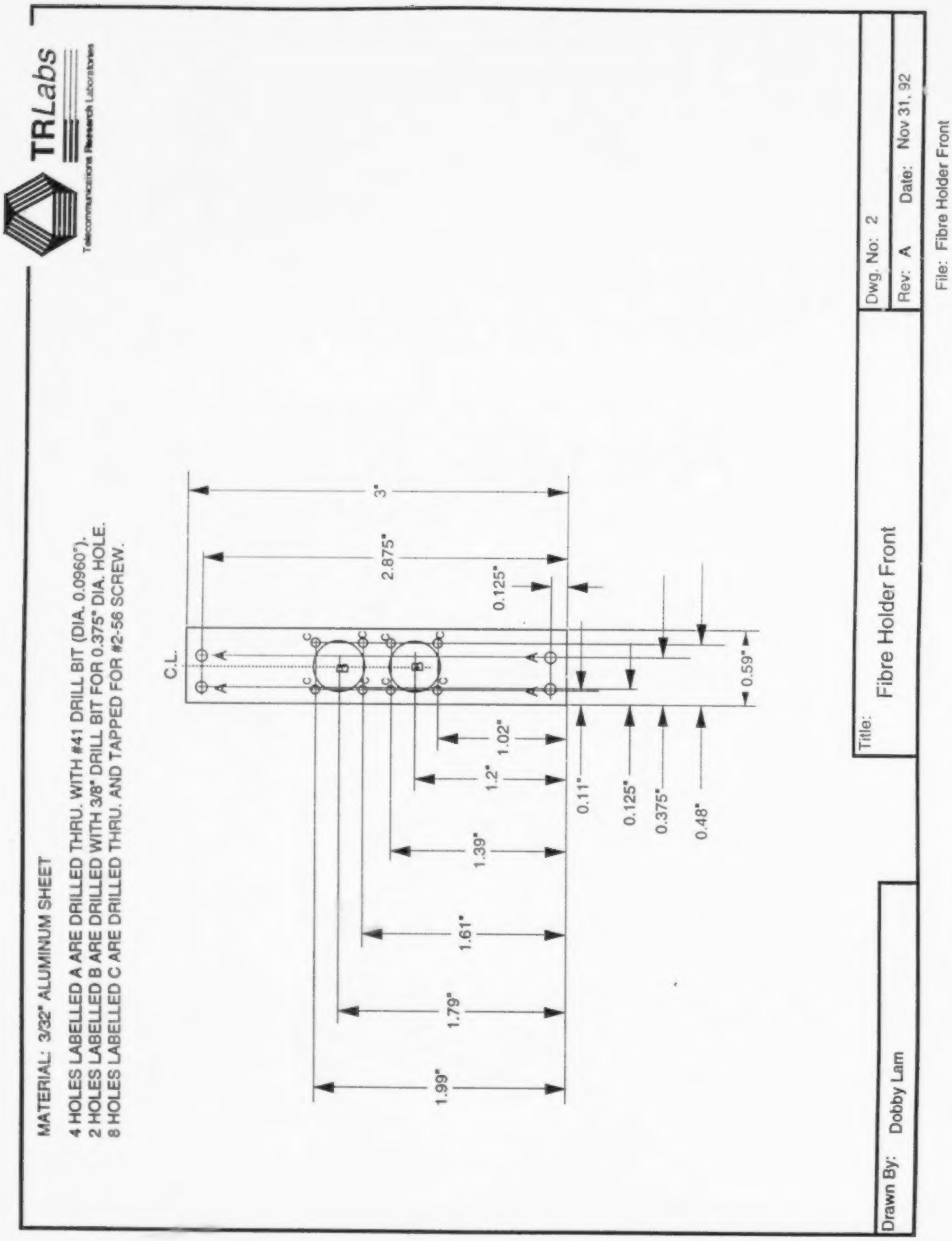

TRLabs
Telecommunications Research Laboratories
MATERIAL: 3/32" ALUMINUM SHEET
4 HOLES LABELLED A ARE DRILLED THRU. WITH #41 DRILL BIT (DIA. 0.0960").
2 HOLES LABELLED B ARE DRILLED WITH 3/8" DRILL BIT FOR 0.375" DIA. HOLE.
8 HOLES LABELLED C ARE DRILLED THRU. AND TAPPED FOR #2-56 SCREW.
C.L.
A
B
C
3"
2.875"
0.125"
0.59"
1.02"
1.2"
1.39"
1.61"
1.79"
1.99"
0.11"
0.125"
0.375"
0.48"
Title:
Fibre Holder Front
Dwg. No: 2
Rev: A
Date: Nov 31, 92
File: Fibre Holder Front
Drawn By: Dobby Lam

Figure F.5 Fiber holder front design

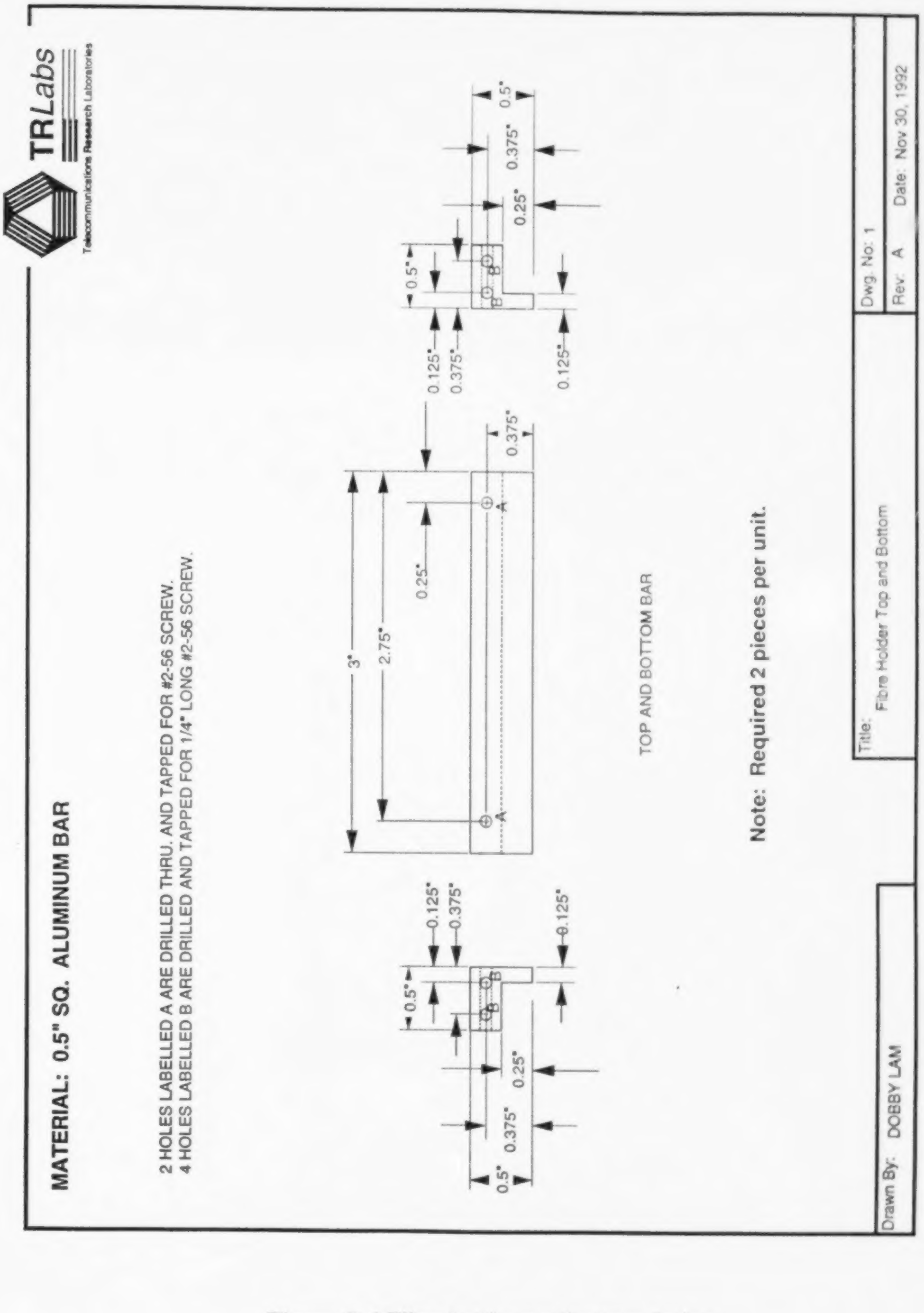

TRLabs
Telecommunications Research Laboratories
MATERIAL: 0.5" SQ. ALUMINUM BAR
2 HOLES LABELLED A ARE DRILLED THRU. AND TAPPED FOR #2-56 SCREW.
4 HOLES LABELLED B ARE DRILLED AND TAPPED FOR 1/4" LONG #2-56 SCREW.
3"
2.75"
0.25"
0.375"
0.125"
0.375"
0.125"
0.5"
0.25"
0.375"
0.5"
A
B
TOP AND BOTTOM BAR
Note: Required 2 pieces per unit.
Drawn By: DOBBY LAM
Title: Fibre Holder Top and Bottom
Dwg. No: 1
Rev: A
Date: Nov 30, 1992
File: Fibre holder top/bottom

Figure F.6 Fiber holder top/bottom design

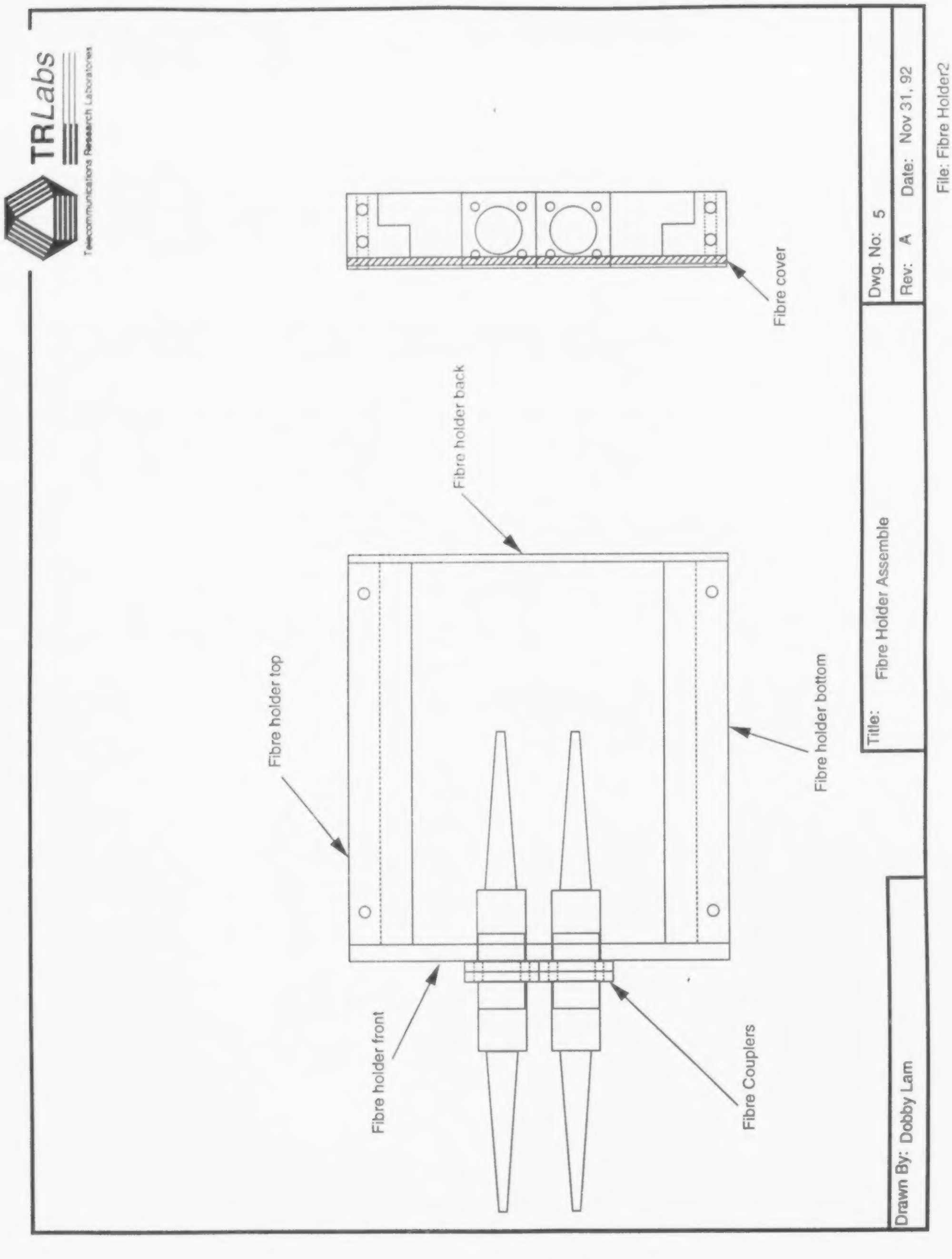

TRLabs
Telecommunications Research Laboratories
Fibre cover
Fibre holder back
Fibre holder top
Fibre holder bottom
Fibre holder front
Fibre Couplers
Title: Fibre Holder Assemble
Dwg. No: 5
Rev: A
Date: Nov 31, 92
File: Fibre Holder2
Drawn By: Dobby Lam

Figure F.7 Fiber holder assembly diagram

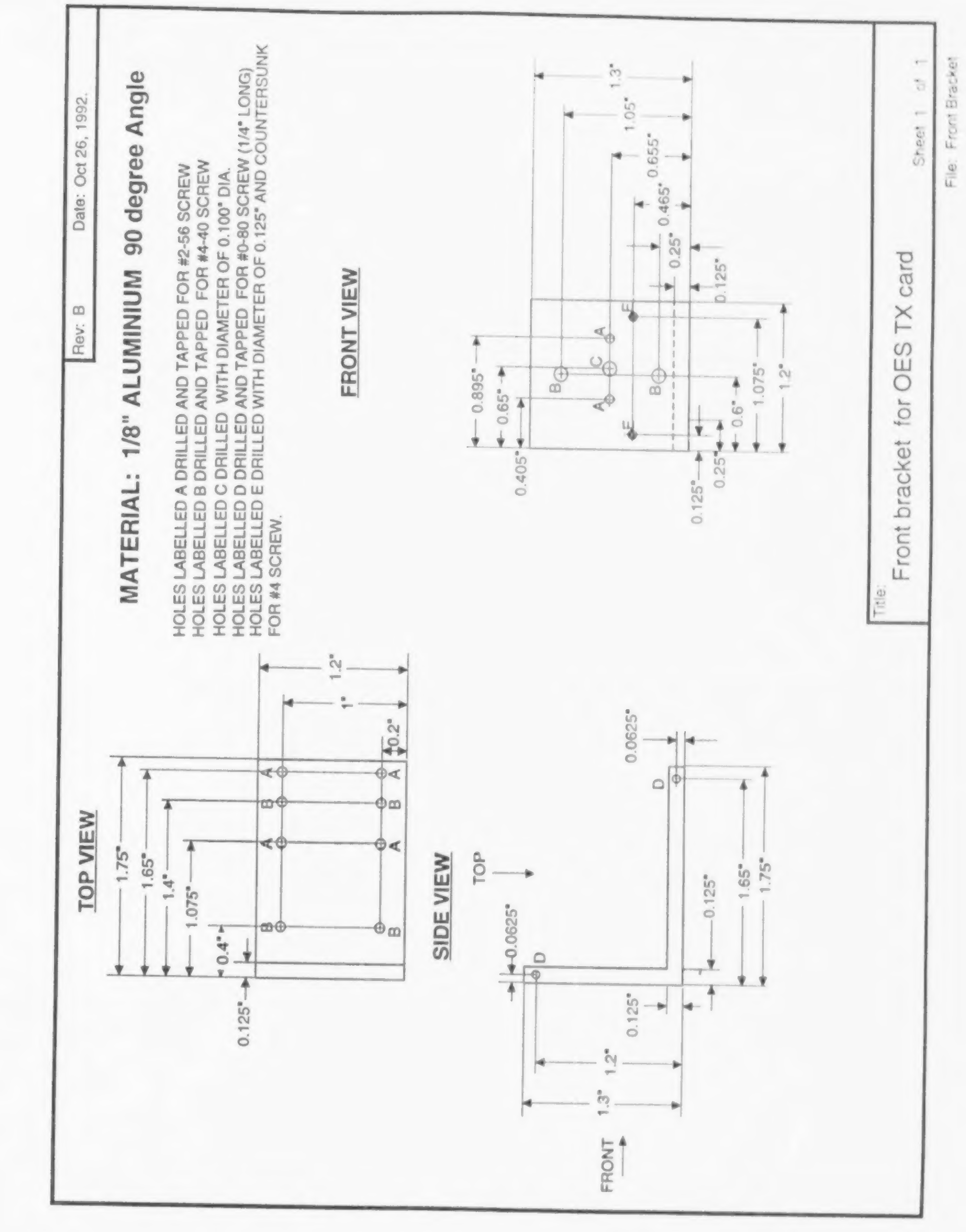
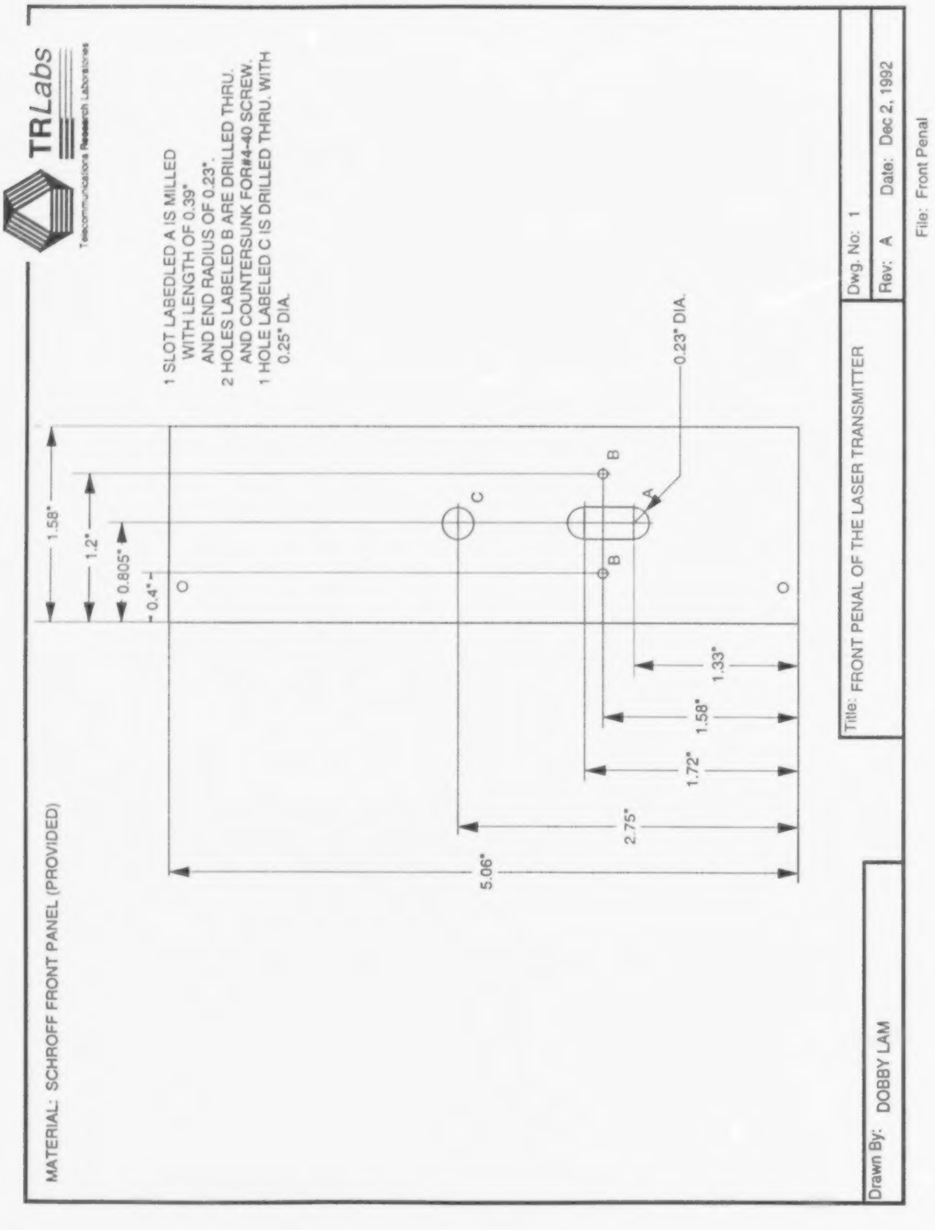

Rev: B
Date: Oct 26, 1992.
MATERIAL: 1/8" ALUMINIUM 90 degree Angle
HOLES LABELLED A DRILLED AND TAPPED FOR #2-56 SCREW
HOLES LABELLED B DRILLED AND TAPPED FOR #4-40 SCREW
HOLES LABELLED C DRILLED WITH DIAMETER OF 0.100" DIA.
HOLES LABELLED D DRILLED AND TAPPED FOR #0-80 SCREW (1/4" LONG)
HOLES LABELLED E DRILLED WITH DIAMETER OF 0.125" AND COUNTERSUNK FOR #4 SCREW.
FRONT VIEW
0.895"
0.65"
0.405"
0.125"
0.25"
0.6"
1.075"
1.2"
1.3"
1.05"
0.655"
0.465"
0.25"
0.125"
A
B
C
D
E
TOP VIEW
1.75"
1.65"
1.4"
1.075"
0.4"
0.125"
1.2"
1"
0.2"
SIDE VIEW
TOP
FRONT
0.0625"
0.125"
1.65"
1.75"
1.2"
1.3"
Title:
Front bracket for OES TX card
Sheet 1 of 1
File: Front Bracket

Figure F.8 Laser mount front bracket design


TRLabs
Telecommunications Research Laboratories
1.58"
1.2"
0.805"
0.4"
C
B
A
B
0.23" DIA.
1.33"
1.58"
1.72"
2.75"
5.06"

MATERIAL: SCHROFF FRONT PANEL (PROVIDED)

1 SLOT LABEDLED A IS MILLED
WITH LENGTH OF 0.39"
AND END RADIUS OF 0.23".
2 HOLES LABELED B ARE DRILLED THRU.
AND COUNTERSINK FOR#4-40 SCREW.
1 HOLE LABELED C IS DRILLED THRU. WITH
0.25" DIA.

Drawn By: DOBBY LAM

Title: FRONT PENAL OF THE LASER TRANSMITTER

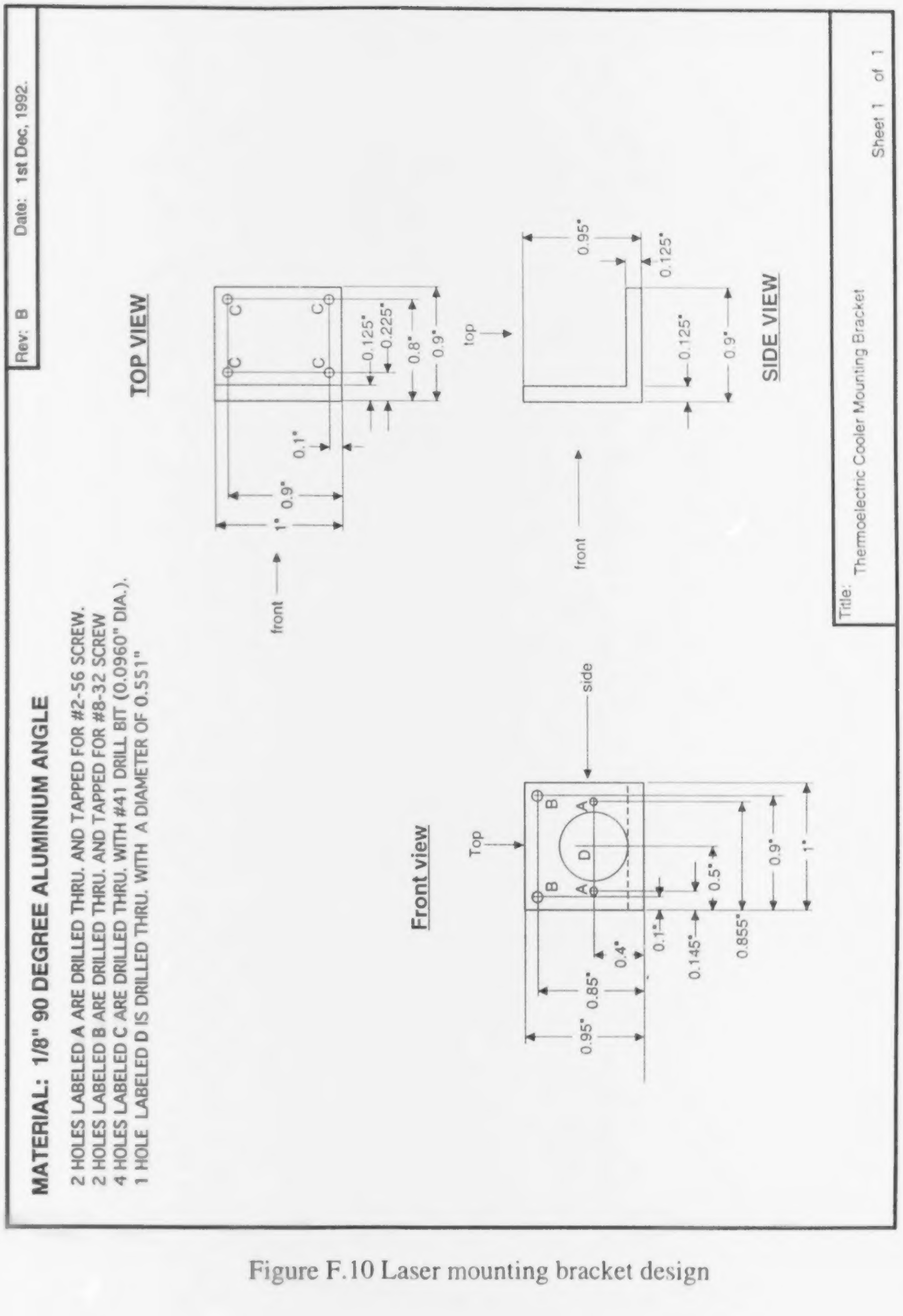
Dwg. No: 1

Rev: A

Date: Dec 2, 1992

File: Front Penal

Figure F.9 Transmitter front panel design



MATERIAL: 1/8" 90 DEGREE ALUMINIUM ANGLE

2 HOLES LABELED A ARE DRILLED THRU. AND TAPPED FOR #2-56 SCREW.
2 HOLES LABELED B ARE DRILLED THRU. AND TAPPED FOR #8-32 SCREW
4 HOLES LABELED C ARE DRILLED THRU. WITH #41 DRILL BIT (0.0960" DIA.).
1 HOLE LABELED D IS DRILLED THRU. WITH A DIAMETER OF 0.551"

Rev: B
Date: 1st Dec, 1992.
Front view
Top
side
A
B
D
0.95"
0.85"
0.4"
0.1"
0.145"
0.855"
0.5"
0.9"
1"
TOP VIEW
front
C
1"
0.9"
0.1"
0.125"
0.225"
0.8"
0.9"
SIDE VIEW
top
front
0.95"
0.125"
0.125"
0.9"
Title:
Thermoelectric Cooler Mounting Bracket
Sheet 1 of 1
File: Laser mounting bracket

Figure F.10 Laser mounting bracket design

Appendix G The Circuit Diagrams of the Receiver Module.

This appendix contains the circuit digrams and printed circuit board design of the receiver module.

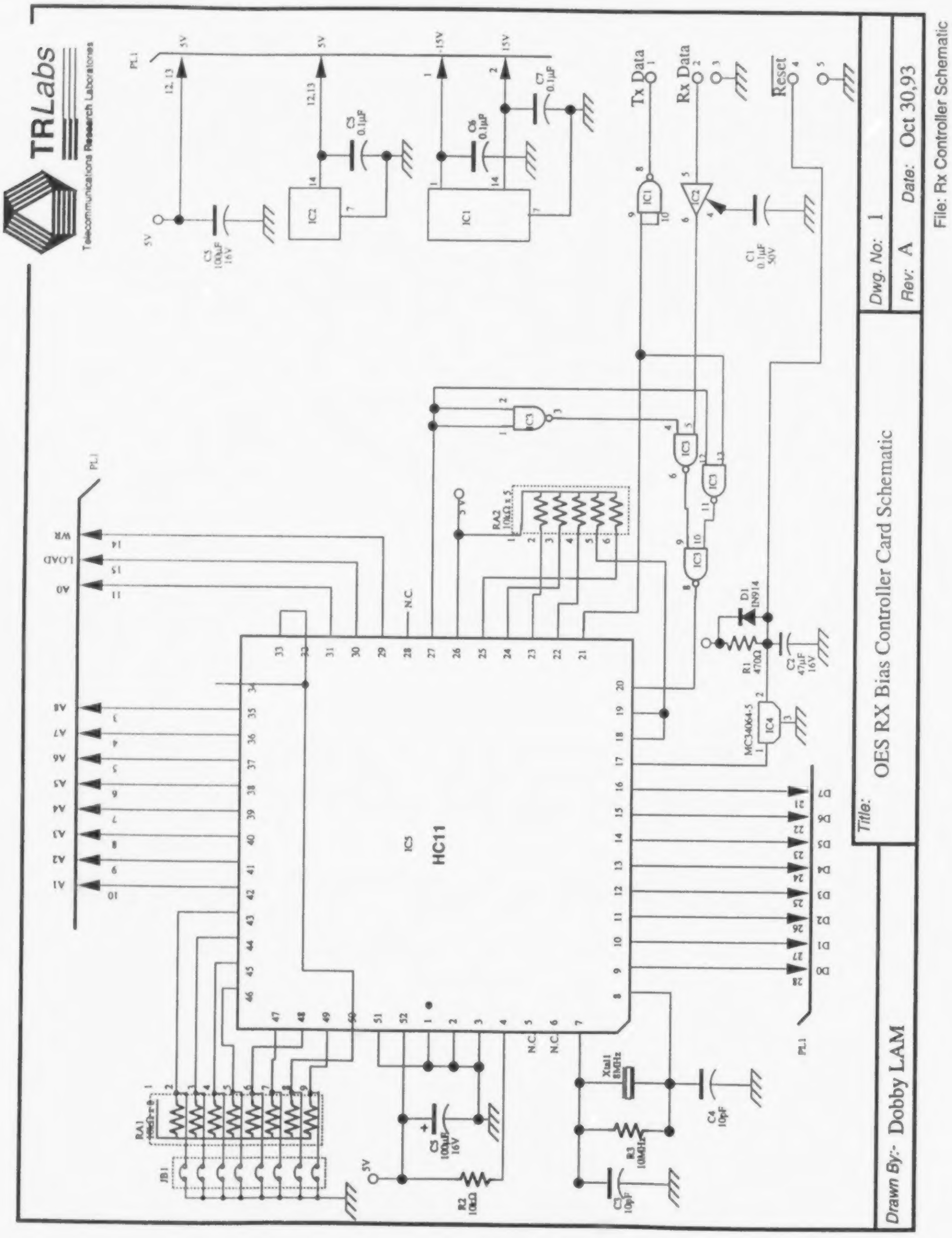

TRLabs
Telecommunications Research Laboratories
Title:
OES RX Bias Controller Card Schematic
Dwg. No: 1
Rev: A
Date: Oct 30,93
Drawn By:- Dobby LAM
File: Rx Controller Schematic
IC5
HC11
Tx Data
Rx Data
Reset
5V
15V
-15V
PL1
IC1
IC2
IC3
IC4
MC34064-5
D1
1N914
R1
470Ω
C1
0.1µF
50V
C2
47µF
16V
C3
100µF
16V
C4
10pF
C5
0.1µF
C6
0.1µF
C7
0.1µF
R2
10kΩ
R3
10MΩ
Xtal1
8MHz
RA1
RA2
10kΩ x 5
JB1
N.C.
A0
LOAD
WR
A1
A2
A3
A4
A5
A6
A7
A8
D0
D1
D2
D3
D4
D5
D6
D7

Figure G.1 The circuit of the Interface Card

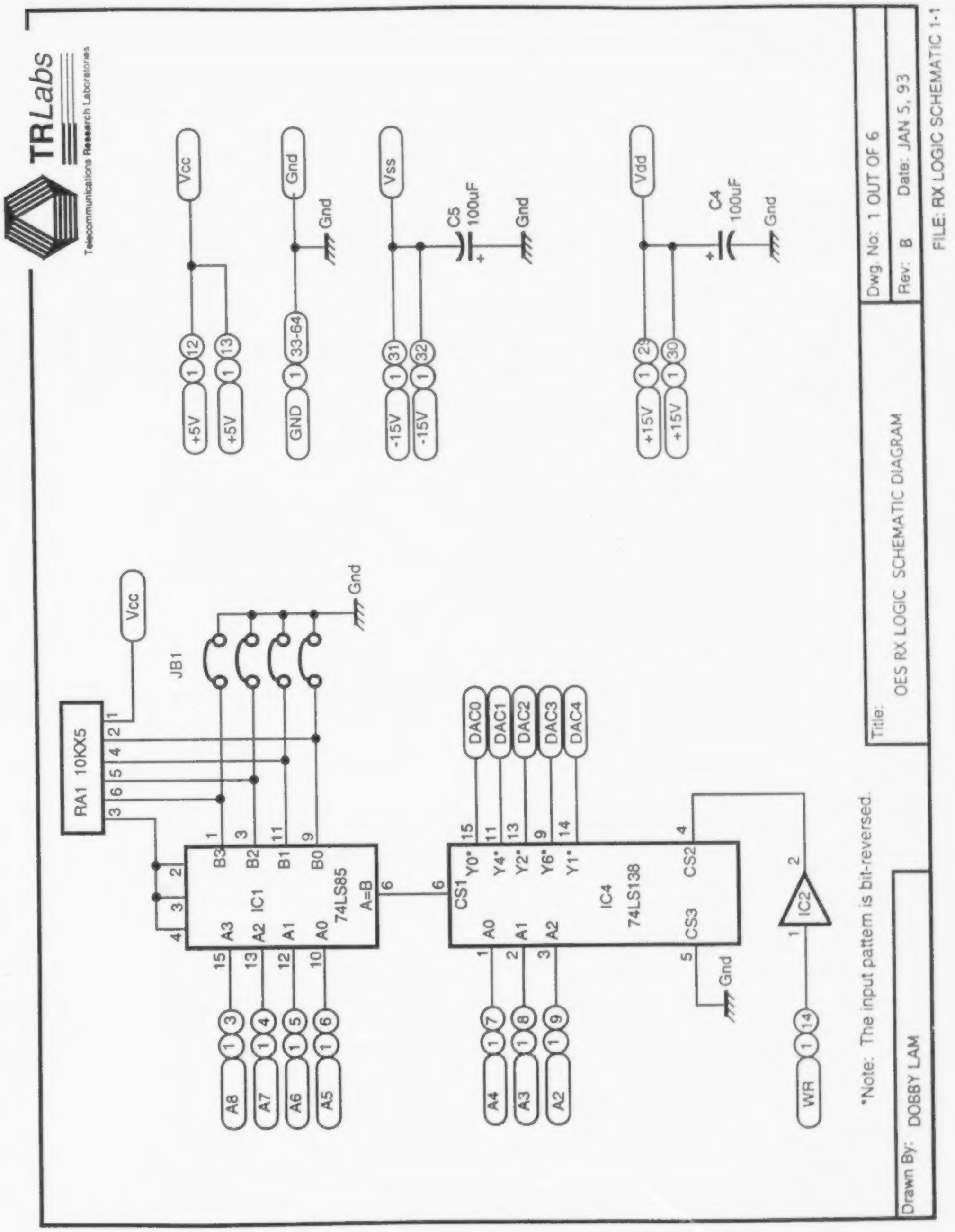

TRLabs
Telecommunications Research Laboratories
RA1 10KX5
Vcc
JB1
Gnd
74LS85
IC1
A=B
74LS138
IC4
CS1
CS2
CS3
Y0*
Y4*
Y2*
Y6*
Y1*
DAC0
DAC1
DAC2
DAC3
DAC4
A8
A7
A6
A5
A4
A3
A2
WR
IC2
+5V
GND
-15V
+15V
Vss
Vdd
C5 100uF
C4 100uF
33-64
*Note: The input pattern is bit-reversed.
Drawn By: DOBBY LAM
Title: OES RX LOGIC SCHEMATIC DIAGRAM
Dwg. No: 1 OUT OF 6
Rev: B
Date: JAN 5, 93
FILE: RX LOGIC SCHEMATIC 1-1

Figure G.2 The circuit of the receiver card (1 out 6)

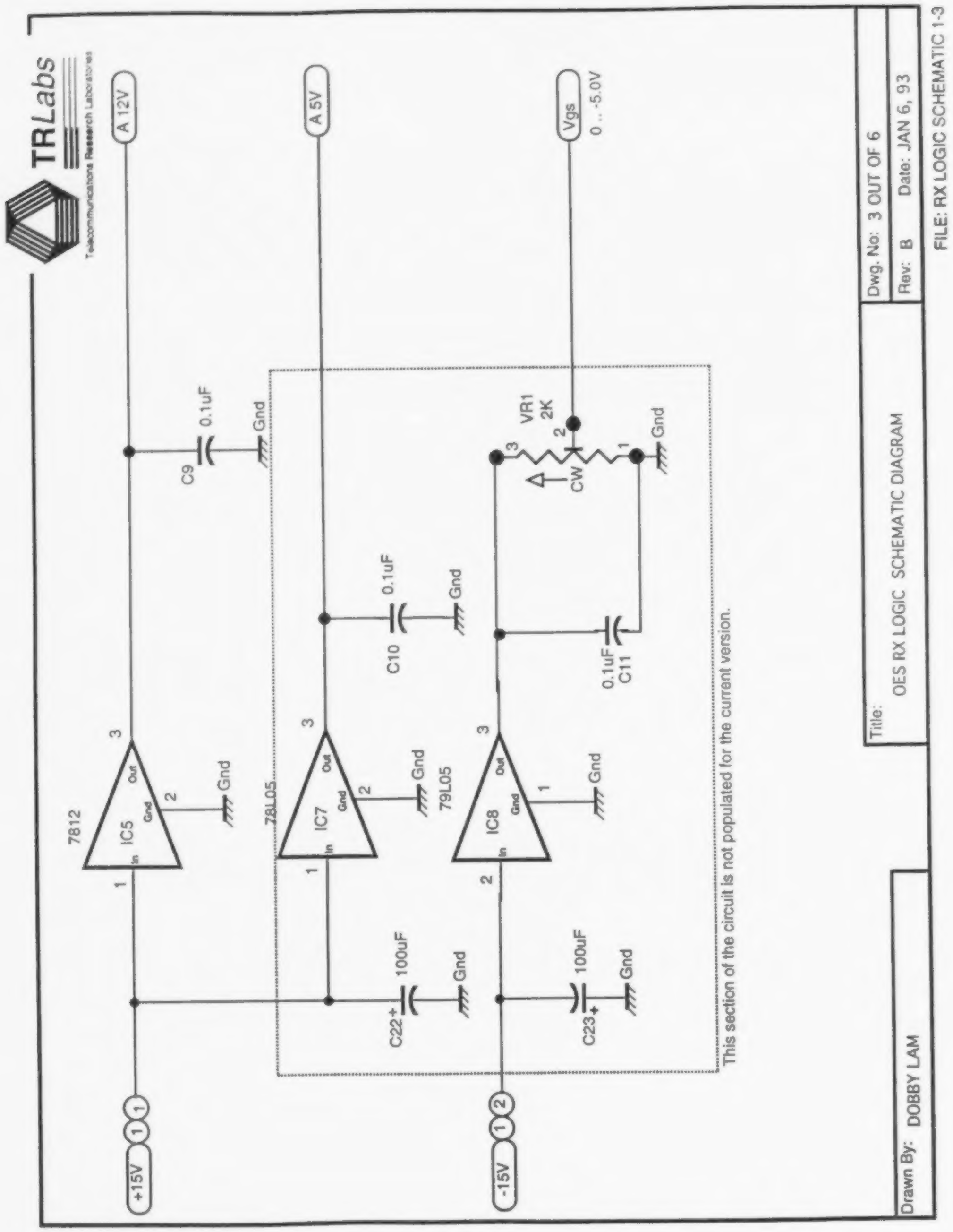

TRLabs
Telecommunications Research Laboratories
A 12V
A 5V
Vgs
0 .. -5.0V
C9
0.1uF
Gnd
VR1
2K
CW
3
2
1
C10
0.1uF
Gnd
0.1uF
C11
7812
IC5
In
Out
Gnd
78L05
IC7
79L05
IC8
+15V
1
1
-15V
1
2
C22+
100uF
C23+
100uF
This section of the circuit is not populated for the current version.
Dwg. No: 3 OUT OF 6
Rev: B
Date: JAN 6, 93
FILE: RX LOGIC SCHEMATIC 1-3
Title:
OES RX LOGIC SCHEMATIC DIAGRAM
Drawn By: DOBBY LAM

Figure G.2 The circuit of the receiver card (2 out 6)

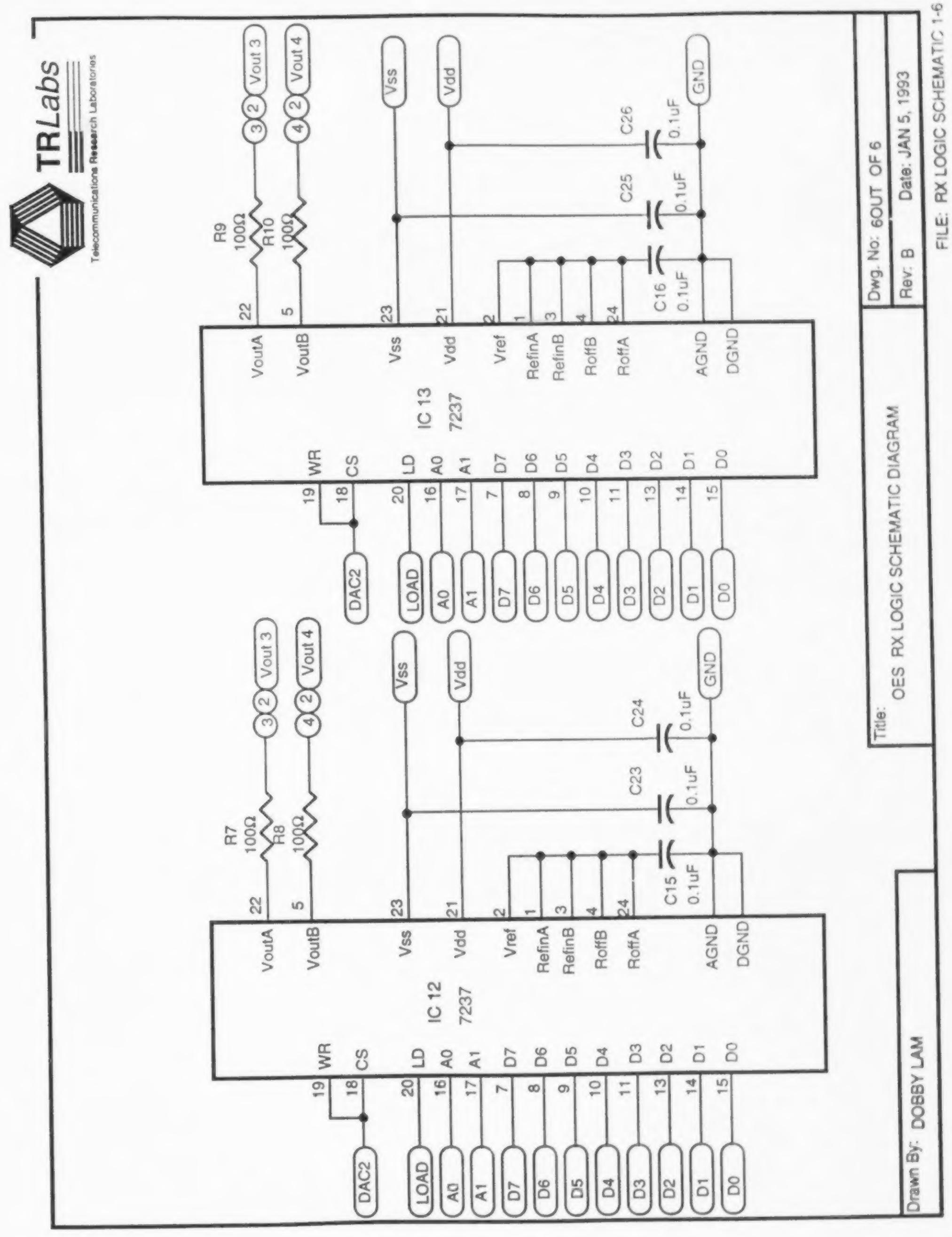
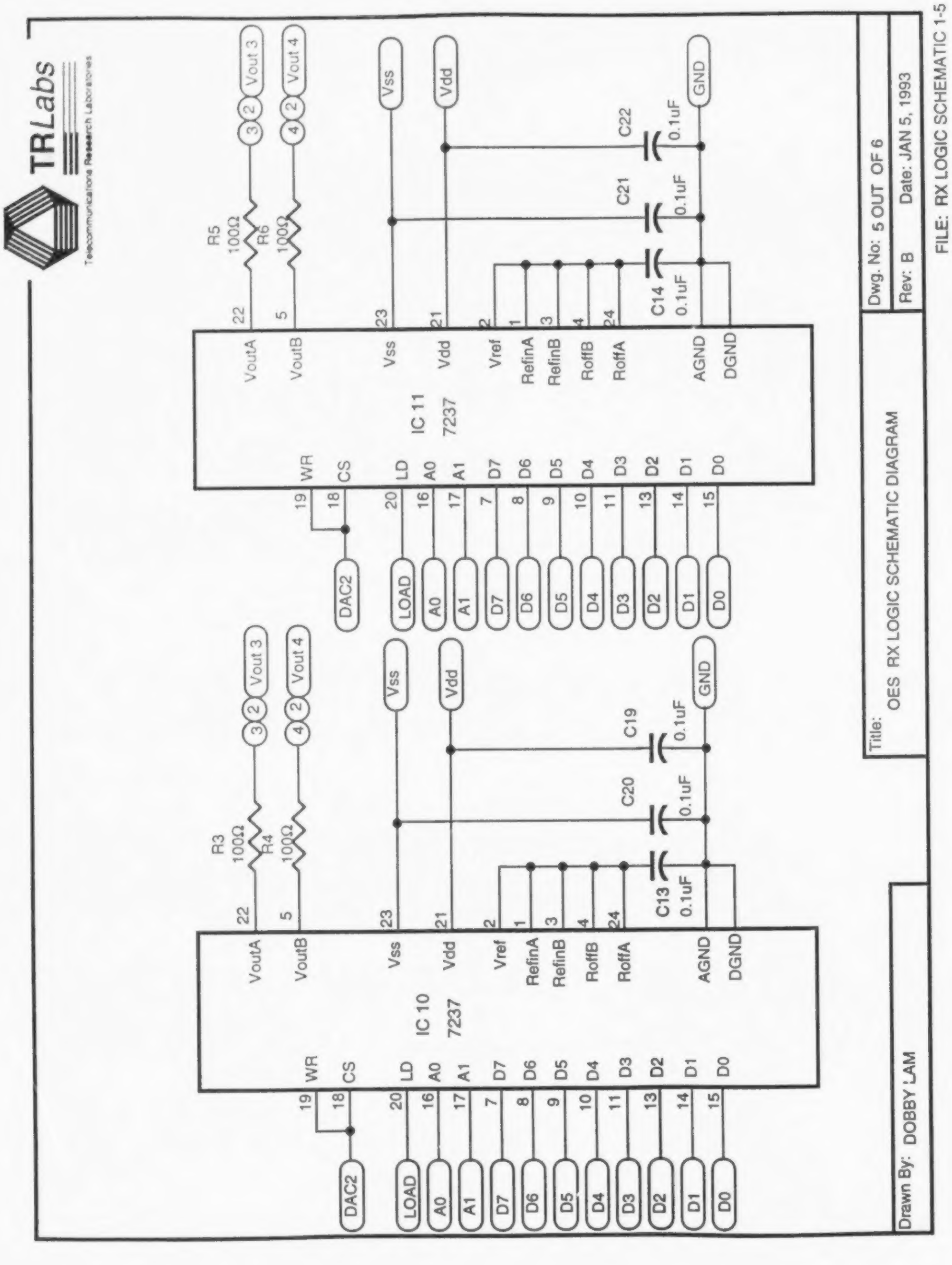

TRLabs
Telecommunications Research Laboratories
IC 12
7237
IC 13
7237
WR
CS
LD
A0
A1
D7
D6
D5
D4
D3
D2
D1
D0
VoutA
VoutB
Vss
Vdd
Vref
RefinA
RefinB
RoffB
RoffA
AGND
DGND
DAC2
LOAD
R7
100Ω
R8
100Ω
R9
100Ω
R10
100Ω
Vout 3
Vout 4
C15
C16
C23
C24
C25
C26
0.1uF
GND
Dwg. No: 6OUT OF 6
Rev: B
Date: JAN 5, 1993
Title:
OES RX LOGIC SCHEMATIC DIAGRAM
Drawn By: DOBBY LAM
FILE: RX LOGIC SCHEMATIC 1-6

Figure G.2 The circuit of the receiver card (3 out 6)



TRLabs
Telecommunications Research Laboratories
R5
100Ω
R6
100Ω
R3
100Ω
R4
100Ω
3
2
Vout 3
4
2
Vout 4
Vss
Vdd
GND
C22
0.1uF
C21
0.1uF
C14
0.1uF
C19
0.1uF
C20
0.1uF
C13
0.1uF
IC 11
7237
IC 10
7237
VoutA
VoutB
Vss
Vdd
Vref
RefinA
RefinB
RoffB
RoffA
AGND
DGND
WR
CS
LD
A0
A1
D7
D6
D5
D4
D3
D2
D1
D0
22
5
23
21
2
1
3
4
24
19
18
20
16
17
7
8
9
10
11
13
14
15
DAC2
LOAD
A0
A1
D7
D6
D5
D4
D3
D2
D1
D0
Drawn By: DOBBY LAM
Title:
OES RX LOGIC SCHEMATIC DIAGRAM
Dwg. No: 5 OUT OF 6
Rev: B
Date: JAN 5, 1993
FILE: RX LOGIC SCHEMATIC 1-5

Figure G.2 The circuit of the receiver card (4 out 6)

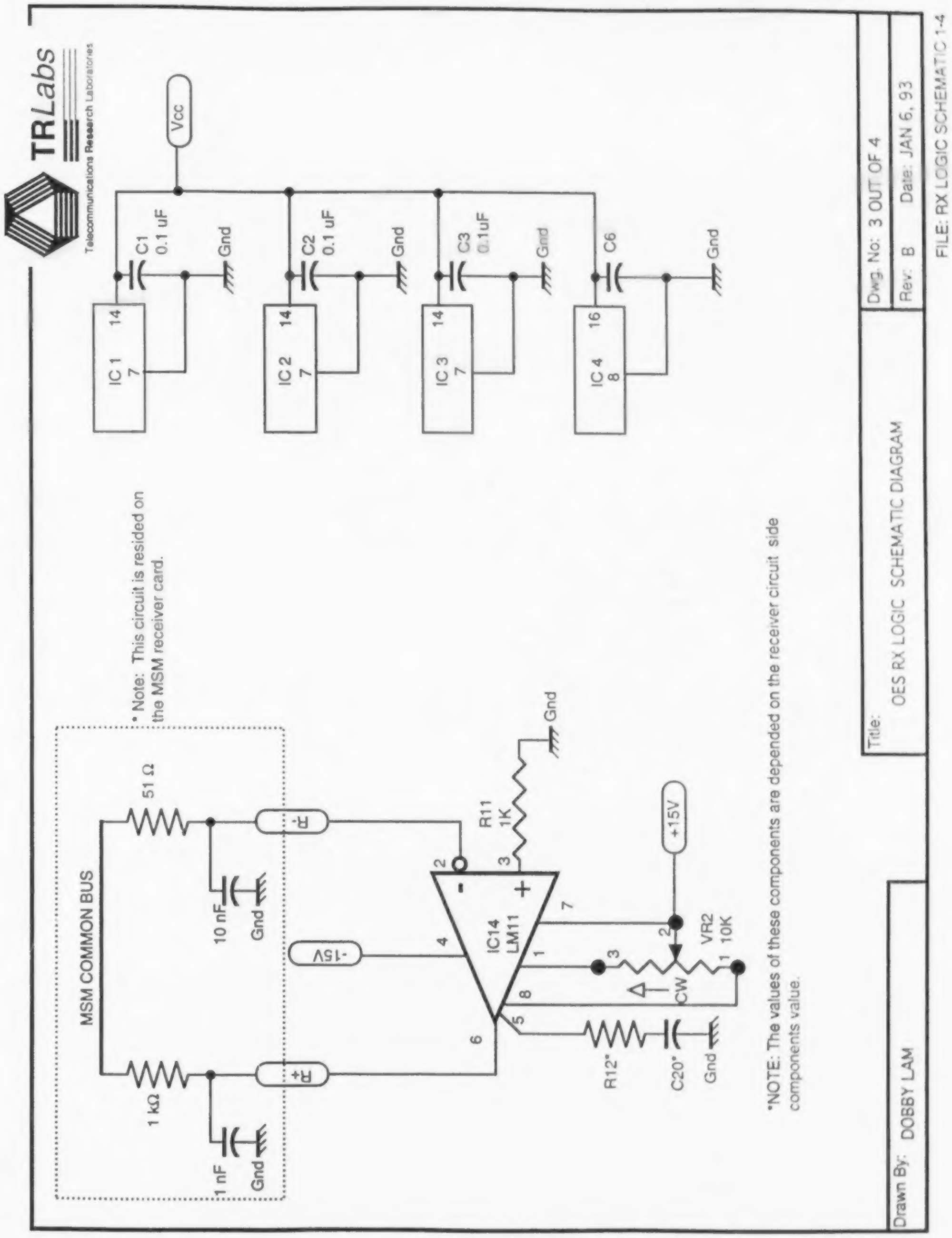

TRLabs
Telecommunications Research Laboratories
Vcc
IC 1 14 7
C1 0.1 uF
Gnd
IC 2 14 7
C2 0.1 uF
Gnd
IC 3 14 7
C3 0.1uF
Gnd
IC 4 16 8
C6
Gnd
* Note: This circuit is resided on the MSM receiver card.
MSM COMMON BUS
51 Ω
10 nF
Gnd
1 kΩ
1 nF
Gnd
R-
R+
-15V
IC14 LM11
2 3 4 6 5 8 1 7
R11 1K
Gnd
+15V
VR2 10K
CW
R12*
C20*
Gnd
*NOTE: The values of these components are depended on the receiver circuit side components value.
Drawn By: DOBBY LAM
Title: OES RX LOGIC SCHEMATIC DIAGRAM
Dwg. No: 3 OUT OF 4
Rev: B
Date: JAN 6, 93
FILE: RX LOGIC SCHEMATIC 1-4

Figure G.2 The circuit of the receiver card (5 out 6)

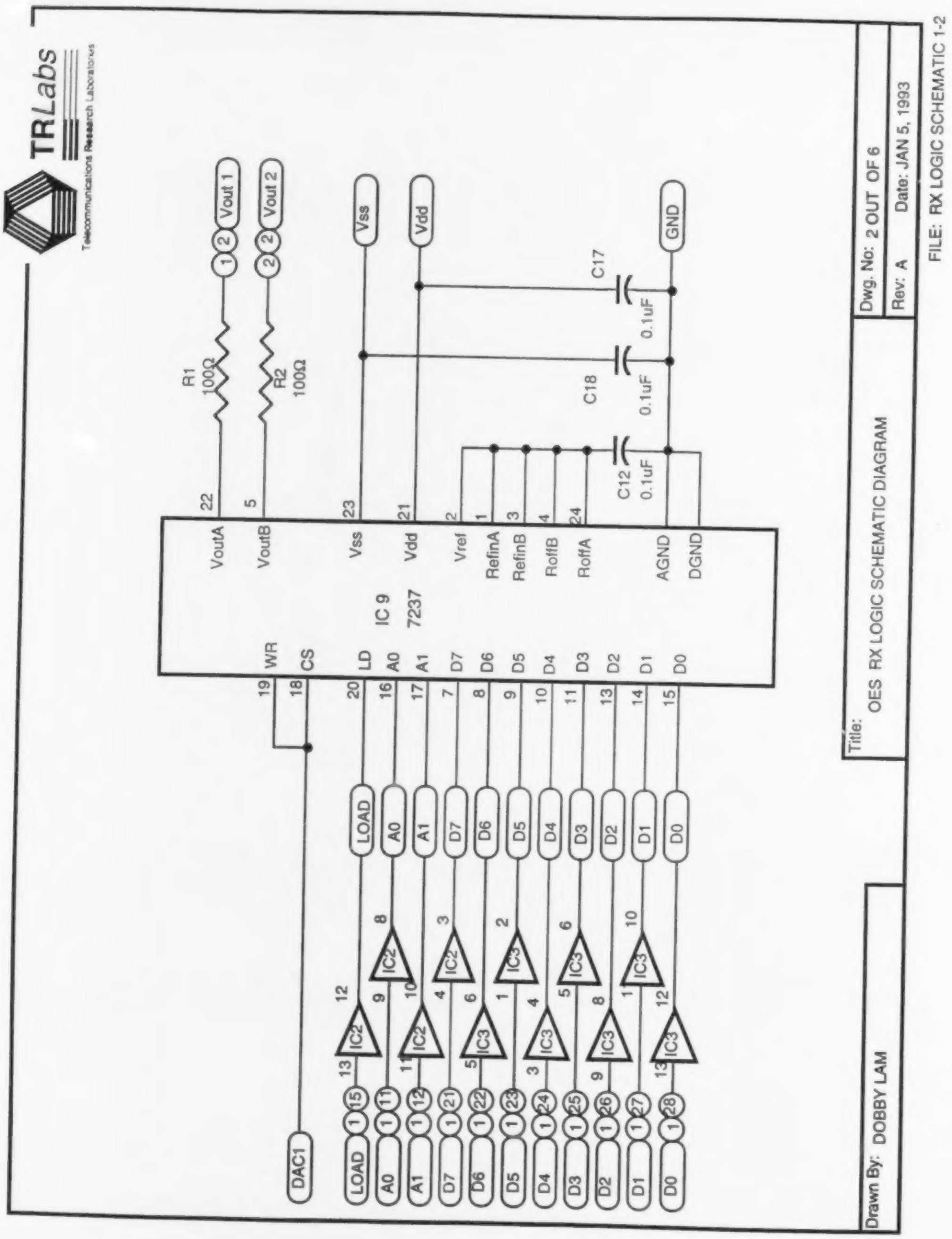

TRLabs
Telecommunications Research Laboratories
Vout 1
Vout 2
Vss
Vdd
GND
R1
100Ω
R2
100Ω
C17
C18
C12
0.1uF
0.1uF
0.1uF
IC 9
7237
VoutA
VoutB
Vss
Vdd
Vref
RefinA
RefinB
RoffB
RoffA
AGND
DGND
WR
CS
LD
A0
A1
D7
D6
D5
D4
D3
D2
D1
D0
IC2
IC3
DAC1
LOAD
A0
A1
D7
D6
D5
D4
D3
D2
D1
D0
Title:
OES RX LOGIC SCHEMATIC DIAGRAM
Dwg. No: 2 OUT OF 6
Rev: A
Date: JAN 5, 1993
FILE: RX LOGIC SCHEMATIC 1-2
Drawn By: DOBBY LAM

Figure G.2 The circuit of the receiver card (6 out 6)

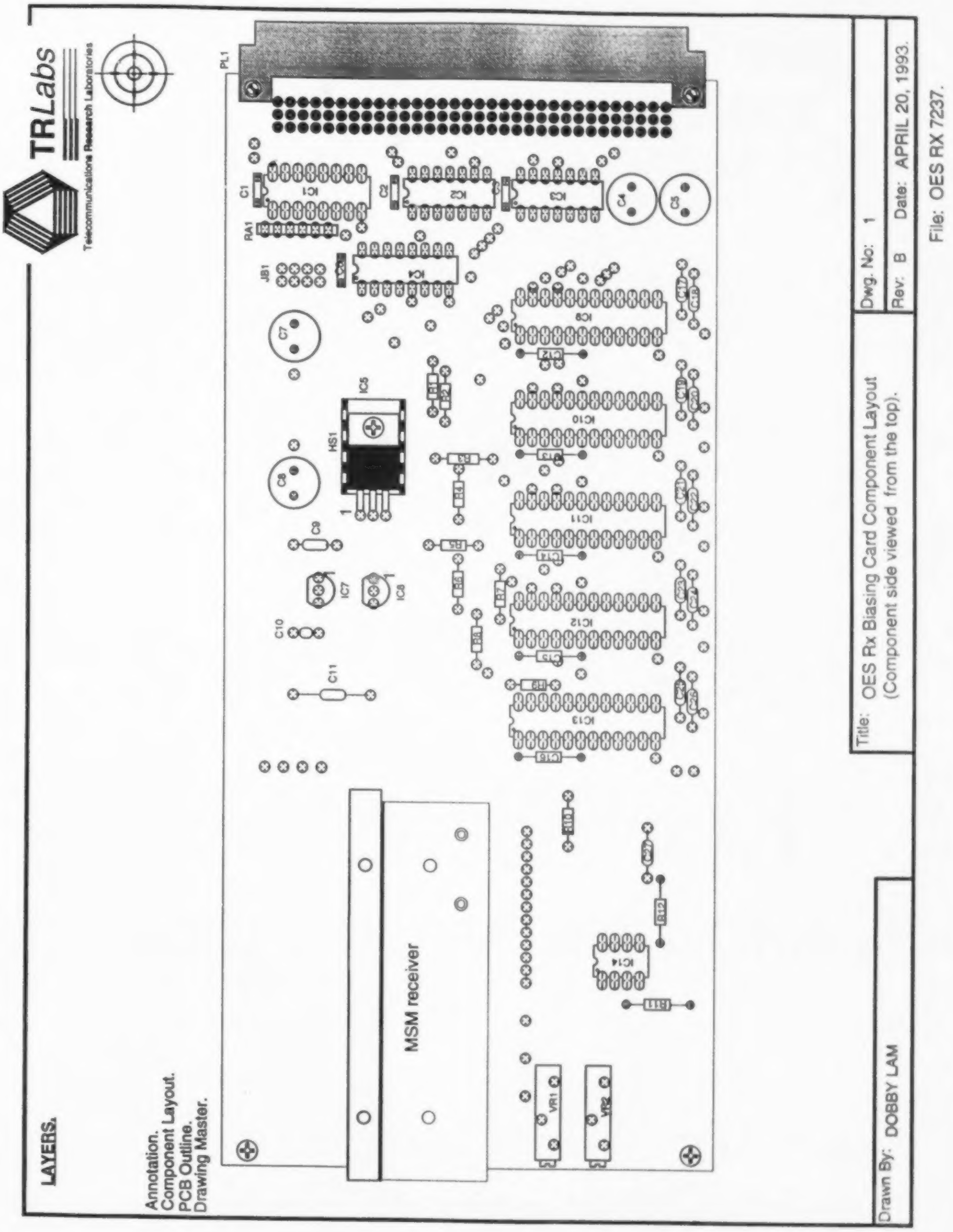
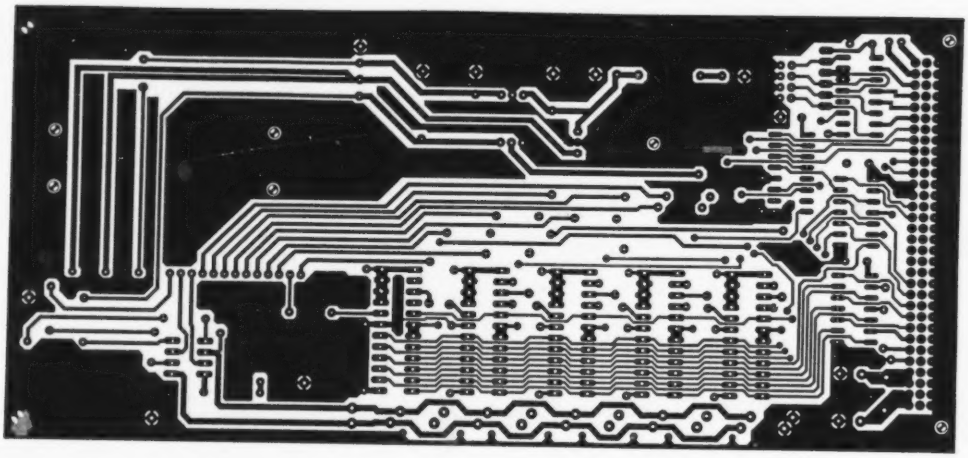
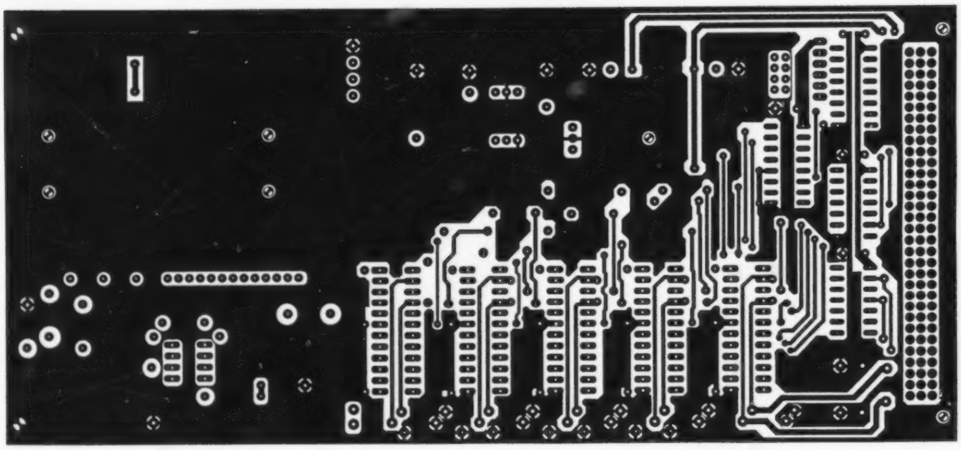

TRLabs
Telecommunications Research Laboratories
LAYERS.
Annotation.
Component Layout.
PCB Outline.
Drawing Master.
PL1
C1
IC1
RA1
JB1
C2
IC2
IC3
IC4
C4
C5
C7
IC5
HS1
C8
1
C9
IC7
IC6
C10
C11
IC8
IC10
IC11
IC12
IC13
IC14
MSM receiver
VR1
VR2
Title: OES Rx Biasing Card Component Layout
(Component side viewed from the top).
Dwg. No: 1
Rev: B
Date: APRIL 20, 1993.
File: OES RX 7237.
Drawn By: DOBBY LAM

Figure G.3 The circuit layout of the receiver card



(a) wiring side



(b) component side

Figure G.4 The circuit board masks of the receiver card

APPENDIX H HC11 INTERNAL EEPROM PROGRAMMING PROCEDURES & RELATED HC11 ASSEMBLE PROGRAM LISTINGS

During the development of this project, a technique was used to program the internal EEPROM of HC11 controller which locates in the memory space of $B600-B7FF. The code to program the EEPROM is provided by Motorola [57] and is listed in List H.1. This code segment is incorporated into the programs, and EEPROIX.ASM, to program the internal EEPROM of HC11 using Motorola HC11EVB evaluation kit and the interface card, respectively.

LISTING H.1 HC11 internal EEPROM programming code

```
*********************************************************
* EEPROG -- program the content of Accumulator A in an EEPROM
*             location stored in stack point Y.
*
* Input:  Acc A = new content of the EEPROM location.
*         Acc B = new content of the EEPROM location.
*         X     = Address pointer of the control register page.
*         Y     = Address pointer of the EEPROM location.
*
* modified: (Y)
*********************************************************
EEPROG          EQU             *
                STAA            PRROG,X
                STAB            ,Y
                INC             PPROG,X
                PSHX
                LDS             #ms10           ;10 ms delay
WAIT2           DEX
                BNE             WAIT2
                PULX
                DEC             PPROG,X         ; set the Erase bit on PFROG
                CLR             PPROG,X
                RTS
```

The setup to program HC11 using a Motorola HC11EVB evaluation kit is shown in Figure H.1.a. Once the connections are secured, execute the following steps to program the EEPROM:

1) Compile and the target program using AS11.EXE. Ensure no errors during compiiing and the target program fit within the EEPROM memory space.
2) Run KERMIT program with a 9600 baud rate.
3) Connect serial port (COM1:) of the IBM personal computer (PC) to the terminal port of HC11EVB.
4) Type CONNECT in the KERMIT environment to connect to the HC11EVB.
5) Type LOAD T<CR> to start the download sequence:
-> type "^] C" to switch back to KERMIT environment
-> type "type eeprogix.s12 > com1:" to type down load the S-record of the program.
6) Type "connect <CR>" to switch back to HC11EVB environment and the ">" prompt should be back on the screen.
7) Type "G C000 <CR>" to execute EEPROGIX.
8) Type "^] C" to switch back to KERMIT environment.
9) Connect COM1: to the host port of the HC11EVB via a null modem cable.
10) Exit KERMIT by typing "exit".

10) Type "stype <CR>" and "[target file name].s19 > com1:" to download the target program into the EEPROM.

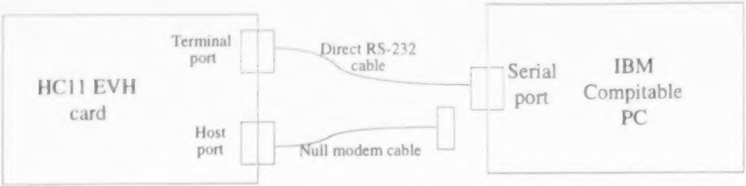


Figure H.1 The connection for the EEPROM programming setup with HC11EVH.

The following listings are the assembly programs for programming the HC11 and for controlling the interfacing card.

Listing H.2 EEPROGIX.ASM (for programming the EEPROM with the HC11EVB)

```
*************************************************************
*                                                                    *
*              This program loads S records form the host to        *
* either a 2864 external EEPROM on the 68HC11 external bus,         *
* or to the 68HC11's internal EEPROM.  It can also be used      *
* verify memory contents against an S record file or just           *
* load RAM located on the 68HC11's external Bus.                *
* Each byte loaded is echoed back to the host.                      *
* When programming a 2864, data polling is used to detect       *
* completion of the programming cycle.                              *
* As the host software always waits for the echo before             *
*                                                                    *
*************************************************************
                PAGE
* Constants
TDRE            EQU             $80
RDRF            EQU             $20
MDA             EQU             $20
SMOD            EQU             $40
ms10            EQU             10000/3
us500           EQU             500/3
*
* Registers
BAUD            EQU             $2B
SCCR1           EQU             $2C
SCCR2           EQU             $2D
SCSR            EQU             $2E
SCDR            EQU             $2F
PPROG           EQU             $3B
HPRIO           EQU             $3C
CONFIG          EQU             $103F
*
* Variables. Notes:  They overwrite initialisation code!!!
                ORG             $C000
EEOPT           RMB             1
MASK            RMB             1
TEMP            RMB             1
LASTBYTE        RMB             1
*
* Program
                ORG             $C000
                LDS             #$FF
                LDX             #$1000
                CLR             SCCR1,X
                LDD             #$300C          Initialize SCI for 8 data bits, 9600 baud
                STAA            BAUD,X
                STAB            SCCR2,X
                BSET            HPRIO,X #MDA
*=>> MAINTAIN SPECTIAL TEST MODE TO ALLOW B96D CONFIG REGISTER PROGRAMING <<=
*               BCLR            HPRIO, X, #$SMOD
ReadOpt         STS             EEOPT
                JSR             READC
                CMPB            #'T'
                BEQ             LOAD
                CMPB            #'X'
                BNE             OptVerf
                INC             EEOPT
                LDAA            #$80
                STAA            MASK
                BRA             LOAD
*
OptVerf         CMPB            #'V'
```

```
                BNE         ReadOpt

                DEC         EEOPT
*
LOAD            EQU         *
                BSR         READC

                CMPB        #'S'
                BNE         LOAD
                BSR         READC
                CMPB        #'1'
                BEQ         LOAD1
                CMPB        #'9'
                BNE         LOAD
                BSR         RDBYTE
                TBA
                SUBA        #2
                BSR         GETADR
LOAD9           BSR         RDBYTE
                DECA
                BNE         LOAD9
                CPY         #0
                BEQ         *
                JMP         ,Y
*
LOAD1           EQU         *
                BSR         RDBYTE
                TBA
                SUBA        #3
                BSR         GETADR
                DEY
                BRA         LOAD1B
*
LOAD1A          LDAB        EEOPT
                BMI         VERIFY
                BEQ         DATAPOLL
                LDAB        #us500
WAIT1           DECB
                BNE         WAIT1
DATAPOLL        LDAB        ,Y
                EORB        LASTBYTE
                ANDB        MASK
                BNE         DATAPOLL
LOAD1E          DECA
                BEQ         LOAD
LOAD1B          BSR         RDBYTE
                INY
                TST         EEOPT
                BMI         LOAD1D
                BEQ         PROG
                STAB        ,Y
LOAD1D          STAB        LASTBYTE
                BRA         LOAD1A
*
VERIFY          LDAB        ,Y
                CMPB        LASTBYTE
                BEQ         LOAD1E
                BSR         WRITEC
                BRA         LOAD1E
*
READC           EQU         *
                BRCLR       SCSR,X #RDRF *
                LDAB        SCDR,X
WRITEC          BRCLR       SCSR,X #TDRE *
                STAB        SCDR,X

                RTS
*
RDBYTE          BSR         READC
                BSR         HEXBIN
                LSLB
                LSLB
                LSLB
                LSLB
                STAB        TEMP
                BSR         READC
                BSR         HEXBIN
                ORAB        TEMP
                RTS
*
GETADR          EQU         *
                PSHA
                BSR         RDBYTE
                TBA
                BSR         RDBYTE
                XGDY
                PULA
                RTS
*
HEXBIN          EQU         *
                CMPB        #'9'
                BLS         HEXNUM
                ADDB            #9
HEXNUM          ANDB            #$F
                RTS
*
PROG            EQU             *
                PSHA
                LDAA            #$16
                CPY             #CONFIG
                BNE             PROGA
                LDAA            #$06
PROGA           BSR             PROGRAM
                LDAA            #2
                BSR             PROGRAM
                CPY             #CONFIG
                BNE             PROGX
                LDAB            ,Y
PROGX           PULA
                BRA             LOAD1D
*
PROGRAM         EQU             *
                STAA            PPROG,X
                STAB            ,Y
                INC             PPROG,X
                PSHX
                LDX             #ms10
WAIT2           DEX
                BNE             WAIT2
                PULX
                DEC             PPROG,X
                CLR             PPROG,X
                RTS
*
                END
```

Listing H.3 CNTRL.ASM (For controlling the interface card).

```
*******************************************************
* EQUATES FOR USE WITH INDEX OFFSET = $100
PORTA           EQU             $00
PACTL           EQU             $28
PORTB           EQU             $04
PORTC           EQU             $03
DDRC            EQU             $07
PORTD           EQU             $08
SPCR            EQU             $28                     (FOR DWOM BIT)
BAUD            EQU             $2B
SCCR1           EQU             $2C
SCCR2           EQU             $2D
SCSR            EQU             $2E
SCDAT           EQU             $2F
PPROG     EQU        $3B
TEST1           EQU             $3E
CONFIG          EQU             $3F

EEPSTR          EQU             $B600                   ;START OF EEPROM
EEPEND          EQU             $B800                   ;END OF EEPROM
RDRF            EQU             $20
TDRE            EQU             $80
DDRA7           EQU             $80
WR_BIT          EQU             $08
A0_BIT          EQU             $04
LD_BIT          EQU             $10
RDY_BIT         EQU             $80

LF              EQU             $0D
CR              EQU             $0A

BUFF            EQU             $00
DATA                            EQU       $08
*****************************************************
                                ORG       $C000

MAIN            EQU             *
* INIT STACK
                LDS   #$FF                     ;RESET STOCK POINTER
* INIT X REG FOR INDEXED ACCESS TO REGISTERS
                LDX             #$1000
                JSR             INIT_SCI
                JSR             INIT_PPI
M1              LDY             #BUFF
                JSR             GET_MESS
                LDAA            BUFF
                CMPA            #'S'
                BNE             M2
                JSR             SET_DAC
M2              CMPA            #'R'
                BNE             M1
                JSR             RE_DAC
                BRA             M1
**********************************************************
```

```
*
* GET_MESS - READ AND ECHO A (MAX 6 CHAR) MESSAGE FROM
*               THE SERIAL PORT.
*
* INPUT: X - I/O SPACE PTR
*            Y - BUFFER SPACE (6 SPACE LONG)
* OUTPUT: (BUFFER) - DATA
*            A      - CHARACTER COUNT
************************************************************
GET_MESS    CLRB
GM1                 BRCLR           SCSR,X RDRF *
                    LDAA            SCDAT,X             ;GET DATA
                    STAA            SCDAT,X             ;ECHO INPUT DATA
                    STAA            0,Y
                    CMPA            #CR                 ;IF CHAR == CR, RETURN
                    BEQ             GM2
                    INY
                    INCB
                    CMPB            #6                  ;IF #CHAR == 6, RETURN
                    BNE             GM1
                    LDAA            #CR
GM2                 STAA            SCDAT,X
                    BRCLR           SCSR,X TDRE *
                    LDAA            #LF
                    STAB            SCDAT,X
                    RTS
************************************************************
*
* INIT_SCI - INITIALIZE SERIAL PORT
*
* INPUT: X - I/O SPACE PTR
*
* OUTPUT: NONE (BUFFER)
*
************************************************************
*
INIT_SCI   EQU       *
* ENABLE HOST PORT (THIS STEP IS ONLY REQUIRED
*  ON THE EVM BOARD ONLY)
*
                    LDAA            #$FF
                    STAA            $4000
* PUT PORT D IN WIRE OR MODE
                    BSET            SPCR,X $20
* ENABLE 8-BIT TRANSMISSION
                    LDAA            #$10
                    STAA            SCCR1,X
* INIT SCI AND RESTART BAUD DIVIDER CHAIN
*  BAUD RATE == 9600
                    LDAA            #$B8                ;DIV BY 13
                    STAA            BAUD,X
* RECEIVER & TRANSMITTER ENABLED
                    LDAA            #$0C
                    STAA            SCCR2,X
                    RTS
************************************************************
*
* INIT_PPI - INITIALIZE ALL FOUR PARALLEL PORTS.
*            PORT A - PA7 SET TO OUTPUT.
*                 BIT 7 - READY BIT (LOW)
*                       BIT 4 - WRITE BIT (HIGH)
*                       BIT 5 - LOAD BIT (HIGH)
*            PORT B - ADDRESS OUTPUT PORT (SET TO $00)
*            PORT C - DATA OUTPUT PORT (SET TO $00)
*            PORT C - WIRE OR INPUT MODE
*
* INPUT: X - I/O SPACE PTR
*
* OUTPUT: NONE
************************************************************
INIT_PPI    BSET    PACTL,X DDRA7
                    BCLR            PORTA,X RDY_BIT|A0_BIT
                    BSET            PORTA,X WR_BIT|LD_BIT
                    CLRA
                    STAA            PORTB,X
                    STAA            PORTC,X
                    LDAA            #$FF
                    STAA            DDRC,X
* PUT PORT D IN WIRE OR MODE
                    BSET            SPCR,X $20
                    RTS
************************************************************
*
* SET_DAC - READ THE ADDRESS AND DATA FROM THE BUFFER
*               AND SET THE DAC PORT ACCORDINGLY.
*
* INPUT: X - I/O SPACE PTR
*            (BUFF) - INPUT MESSAGE.
*
* OUTPUT: NONE
************************************************************
SET_DAC             LDAA            BUFF+1
```

```
                JSR             GET_HEX
                BCS             SD1
                ASLA
                ASLA
                ASLA
                ASLA
                STAA            BUFF
                LDAA            BUFF+2
                JSR             GET_HEX
                BCS             SD1
                ADDA            BUFF
                STAA            BUFF
                LDAA            BUFF+3
                JSR             GET_HEX
                BCS             SD1
                STAA            DATA+1
                LDAA            BUFF+4
                JSR             GET_HEX
                BCS             SD1
                STAA            BUFF
                LDAA            BUFF+5
                JSR             GET_HEX
                BCS             SD1
                LDAA            BUFF
                JSR             WR_DAC
SD1             RTS

GET_HEX         CMPA            #'0'
                BLT             GH1
                CMPA            #'9'
                BLT             GH2
                CMPA            #'A'
                BLT             GH1
                CMPA            #'F'
                BLT             GH3
                CMPA            #'A'
                BLT             GH1
                CMPA            #'F'
                BGT             GH1
                ANDA            #$7F
GH3             SUBA            #'A'-10
                CLC
                RTS
GH2             SUBA            #'0'
                CLC
                RTS
GH1             SEC
                RTS
************************************************************
*
* WR_DAC - WRITE A DATA WORD TO A SPECIFIED DAC PORT.
*
* INPUT: X - I/O SPACE PTR
*            (DATA) - DATA WORD
* OUTPUT: NONE
************************************************************
WR_DAC  STAA    PORTB,X
                LDAA                DATA
                STAA                PORTC,X
                BCLR                PORTA,X WR_BIT
                BSET                PORTA,X WR_BIT
                LDAA                DATA+1
                STAA                PORTC,X
                BSET                PORTA,X A0_BIT
                BCLR                PORTA,X WR_BIT
                BSET                PORTA,X WR_BIT
                BCLR                PORTA,X LD_BIT
                BSET                PORTA,X LD_BIT|A0_BIT
                RTS
************************************************************
* RD_DAC - RESET ALL DAC PORTS TO $800 VALUE.
*
* INPUT: X - I/O SPACE PTR
*            (DATA) - DATA WORD
* OUTPUT: NONE
************************************************************
RE_DAC  CLR     DATA
                LDAA                #$08
                STAA                DATA+1
                LDAA                #$99
RD1             JSR                 SET_DAC
                DECA
                DAA
                CMPA                #$99
                BNE                 RD1
                RTS
```

APPENDIX I THEORETICAL CALCULATION OF THE RESPONSIVITY OF GaAs MSM PHOTODIODE

First, the light is assumed to be totally absorbed within the epitaxial layer; therefore, the absorption depth is not considered. The internal quantum efficient is the rate of charge carrier generation per optical power and is given as:

$$\eta_{in} = {}^{e}\!\big/\!{}_{\frac{hc}{\lambda}} = \frac{e\lambda}{hc} \qquad (\text{I.1}).$$

With a wavelength of 780 nm, the internal quantum efficient is calculated to be 0.629 A/W. The responsivity of a MSM photodiode is less than the internal quantum efficient due to both the shadowing effect of the electrodes and the optical coupling. Form Figure I.1, the electrodes cover a portion of the detector surface and reduce the responsivity with the ratio of open and covered areas. This ratio is given by

$$Ratio_{area} = \frac{s}{s+w} \qquad (\text{I.2})$$

where w is the finger width and s is the finger spacing. There are two possible interfaces between the optical fiber and the MSM photodiode. First, an air gap is leave between the fiber and the MSM surface. This arrangement leads to two reflective surfaces. The coupling efficient is given as [42]

$$\begin{aligned} \eta_{coupling} &= \left(1 - \Re_{air-MSM}\right)\left(1 - \Re_{fiber-air}\right) \\ &= \left(1 - \left(\frac{n_{GaAs} - n_{air}}{n_{GaAs} + n_{air}}\right)^2\right)\left(1 - \left(\frac{n_{air} - n_{fiber}}{n_{air} + n_{fiber}}\right)^2\right) \qquad (\text{I.3}) \end{aligned}$$

where n is the reflective index of the material and R is the reflectance at the interface. In the second case, a reflective index matched material fills the gap between the fiber and the MSM surface. In this case, only reflective interface presents and the coupling efficient is given as [42]

$$\begin{aligned} \eta_{coupling} &= 1 - \Re_{GaAs-fiber} \\ &= 1 - \left(\frac{n_{GaAs} - n_{fiber}}{n_{GaAs} + n_{fiber}}\right)^2 \qquad (\text{I.4}). \end{aligned}$$

The responsivity is given as the product of Eqs. (I.1), (I.4), and (I.2) or (I.3)

$$R = \eta_{internal} \cdot Ratio_{area} \cdot \eta_{coupling}$$

(I.4).

The constants and the material parameters are given as following table

Table I.1 The material parameter for MSM responsivity calculation

Symbols	Value	Unit
h	6.626e-34	Js
c	3.000e8	m/s
n_{GaAs}	3.4	----
n_{air}	1.0	----
n_{fiber}	1.5	----

The responsivities of 1 μm and 3 μm detectors with the two different interfaces are calculated and listed in the following table

Table I.2 The MSM responsivity with different finger spacing and interfaces.

	With index matching	Without index matching
Detector spacing = 1μm	0.26 A/W	0.21 A/W
Detector spacing = 3μm	0.4 A/W	0.31 A/W